

Service Manual

Reference No. : SM- PDP42AAMIA1SS -001

Revision : 0

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Page : P.1 of 103

In House Model No. : PDP42EAA

Customer Model No. : PPP4206EM1

BOM No : PDP42AAMIA1SS -A01

Description : Service Manual for PDP4206EM1_SDI V4 USA

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SERVICE MANUAL

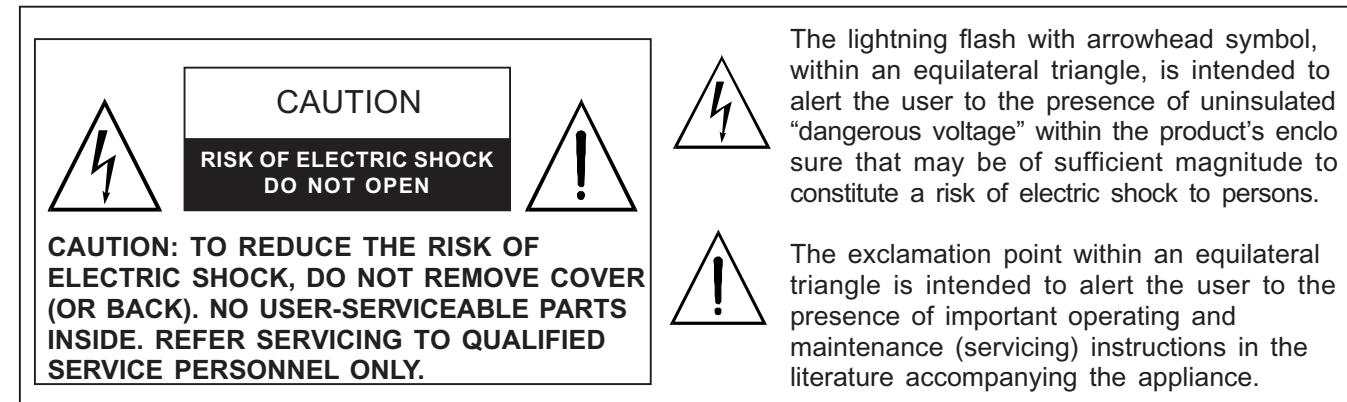
Model:

PDP4206EM1

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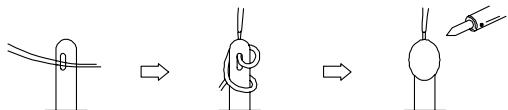
This manual is the latest at the time of printing, and does not include the modification which may be made after the printing, by the constant improvement of product.

Safety Precaution



PRECAUTIONS DURING SERVICING

1. In addition to safety, other parts and assemblies are specified for conformance with such regulations as those applying to spurious radiation. These must also be replaced only with specified replacements.
Examples: RF converters, tuner units, antenna selection switches, RF cables, noise-blocking capacitors, noise-blocking filters, etc.
2. Use specified internal Wiring. Note especially:
 - 1) Wires covered with PVC tubing
 - 2) Double insulated wires
 - 3) High voltage leads
3. Use specified insulating materials for hazardous live parts. Note especially:
 - 1) Insulating Tape
 - 2) PVC tubing
 - 3) Spacers (insulating barriers)
 - 4) Insulating sheets for transistors
 - 5) Plastic screws for fixing micro switches
4. When replacing AC primary side components (transformers, power cords, noise blocking capacitors, etc.), wrap ends of wires securely about the terminals before soldering.



5. Make sure that wires do not contact heat generating parts (heat sinks, oxide metal film resistors, fusible resistors, etc.)
6. Check if replaced wires do not contact sharply edged or pointed parts.
7. Make sure that foreign objects (screws, solder droplets, etc.) do not remain inside the set.

The lightning flash with arrowhead symbol, within an equilateral triangle, is intended to alert the user to the presence of uninsulated "dangerous voltage" within the product's enclosure that may be of sufficient magnitude to constitute a risk of electric shock to persons.

The exclamation point within an equilateral triangle is intended to alert the user to the presence of important operating and maintenance (servicing) instructions in the literature accompanying the appliance.

MAKE YOUR CONTRIBUTION TO PROTECT THE ENVIRONMENT

Used batteries with the ISO symbol



for recycling as well as small accumulators (rechargeable batteries), mini-batteries (cells) and starter batteries should not be thrown into the garbage can.

Please leave them at an appropriate depot.

WARNING:

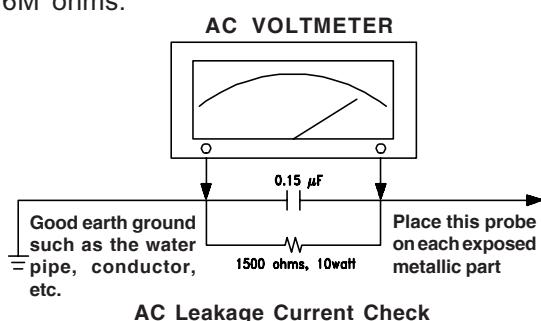
Before servicing this TV receiver, read the SAFETY INSTRUCTION and PRODUCT SAFETY NOTICE.

SAFETY INSTRUCTION

The service should not be attempted by anyone unfamiliar with the necessary instructions on this apparatus. The following are the necessary instructions to be observed before servicing.

1. An isolation transformer should be connected in the power line between the receiver and the AC line when a service is performed on the primary of the converter transformer of the set.
2. Comply with all caution and safety related provided on the back of the cabinet, inside the cabinet, on the chassis or picture tube.
3. To avoid a shock hazard, always discharge the picture tube's anode to the chassis ground before removing the anode cap.
4. Completely discharge the high potential voltage of the picture tube before handling. The picture tube is a vacuum and if broken, the glass will explode.

5. When replacing a MAIN PCB in the cabinet, always be certain that all protective are installed properly such as control knobs, adjustment covers or shields, barriers, isolation resistor networks etc.
6. When servicing is required, observe the original lead dressing. Extra precaution should be given to assure correct lead dressing in the high voltage area.
7. Keep wires away from high voltage or high temperature components.
8. Before returning the set to the customer, always perform an AC leakage current check on the exposed metallic parts of the cabinet, such as antennas, terminals, screwheads, metal overlay, control shafts, etc., to be sure the set is safe to operate without danger of electrical shock. Plug the AC line cord directly to the AC outlet (do not use a line isolation transformer during this check). Use an AC voltmeter having 5K ohms volt sensitivity or more in the following manner. Connect a 1.5K ohm 10 watt resistor paralleled by a 0.15 μ F AC type capacitor, between a good earth ground (water pipe, conductor etc.,) and the exposed metallic parts, one at a time. Measure the AC voltage across the combination of the 1.5K ohm resistor and 0.15 μ F capacitor. Reverse the AC plug at the AC outlet and repeat the AC voltage measurements for each exposed metallic part. The measured voltage must not exceed 0.3V RMS. This corresponds to 0.5mA AC. Any value exceeding this limit constitutes a potential shock hazard and must be corrected immediately. The resistance measurement should be done between accessible exposed metal parts and power cord plug prongs with the power switch "ON". The resistance should be more than 6M ohms.



AC Leakage Current Check

PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in this apparatus have special safety-related characteristics.

These characteristics are offer passed unnoticed by visual inspection and the protection afforded by them cannot necessarily be obtained by using replacement components rates for a higher voltage, wattage, etc.

The replacement parts which have these special safety characteristics are identified by Δ marks on the schematic diagram and on the parts list.

Before replacing any of these components, read the parts list in this manual carefully. The use of substitute replacement parts which do not have the same safety characteristics as specified in the parts list may create shock, fire, or other hazards.

9. Must be sure that the ground wire of the AC inlet is connected with the ground of the apparatus properly.

1. Standard Test Conditions

All tests shall be performed under the following conditions, unless otherwise specified.

- 1.1 Ambient light : 150ux (When measuring I_B , the ambient luminance $\leq 0.1\text{Cd/m}^2$)
- 1.2 Viewing distance : 50cm in front of PDP
- 1.3 Warm up time : 30 minutes
- 1.4 PDP Panel facing : no restricted
- 1.5 Measuring Equipment : PC, Chroma 2225 signal generator (with Chroma digital additional card) or equivalent, Minolta CA100 photometer
- 1.6 Magnetic field : no restricted
- 1.7 Control settings : Brightness, Contrast, Tint, Color set at Center(50)
- 1.8 Power input : 100~120Vac 60Hz
- 1.9 Ambient temperature : $20^\circ\text{C} \pm 5^\circ\text{C}$ ($68^\circ\text{F} \pm 9^\circ\text{F}$)
- 1.10 Display mode : Resolution 852 (H) x 480 (V) Pixels
- 1.11 Other conditions :
 - 1.11.1 With image sticking protection of PDP module, the luminance will descend by time on a same still screen and rapidly go down in 5 minutes. When measuring the color tracking and luminance of a same still screen, be sure to accomplish the measurement in one minute to ensure its accuracy.
 - 1.11.2 Due to the structure of PDP, the extra-high-bright same screen should not hold over 5 minutes for fear of branding on the panel.

Technical Specifications

PDP4206EM1

ELECTRICAL CHARACTERISTICS

2. Power Input

2.1	<u>Voltage</u>	:	100 ~120VAC 60Hz
2.2	<u>Input Current</u>	:	5.0 /2.5A
2.3	<u>Maximum Inrush Current</u>	:	<30 A (FOR AC110V ONLY)
	Test condition	:	Measured when switched off for at least 20 mins
2.4	<u>Frequency</u>	:	60Hz(±3Hz)
2.5	<u>Power Consumption</u>	:	330W Typical
	Test condition	:	full white display with maximum brightness and contrast
2.6	<u>Power Factor</u>	:	Meets IEC1000-3-2
2.7	<u>Withstanding voltage</u>	:	1.5kVac or 2.2kVdc for 1 sec

3. Display

3.1	Screen Size	:	42" Plasma display
3.2	Aspect Ratio	:	16:9
3.3	Pixel Resolution	:	852x480
3.4	Peak Brightness	:	1500 cd/m ² (Typical, Panel only)
3.5	Contrast Ratio (Dark room)	:	10000:1 (Ratio, Typical, in a dark room, Panel only)
3.6	Viewing Angle	:	Over 160°
3.7	OSD language	:	English, French, Spanish.

4. Signal

4.1 AV & Graphic input

4.1.1	Composite signal	:	AV
4.1.2	Y,C Signal	:	S-Video
4.1.3	Component signal	:	YPbPr, HDMI, VGA compatible
4.1.4	Graphic I/P	:	Analog: D-sub 15pin detachable cable Digital:HDMI
4.1.5	EDID compatibility	:	DDC 1.3
4.1.6	I/P frequency	:	f _H : 31.5kHz to 60kHz/f _V : 56.25Hz to 75Hz(1024x768 recommended)

4.2 Audio input	VGA(D-Sub 15 Pin Type)×1 D-Sub 9 Pin (RS-232 Input) × 1 HDMI (Ver. 1.1) connector × 1 S-Video (Mini Din 4 Pin) × 1 Video Input (RCA Type) × 1 YPbPr × 2 Stereo, Audio × 6
4.3 Audio output	Audio&Video Output (RCA Type) × 1, SPDIF(Optical) × 1

PIP/PBP, Picture size, Picture Still, Sound mode,Last
memory, Timer

5. Environment

5.1 Operating environment

5.1.1 Temperature	: 5° to 33°C
5.1.2 Relative humidity	: 20% to 85%(non-condensing)

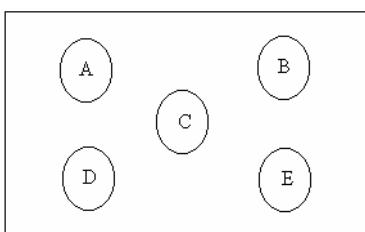
5.2 Storage and Transport

5.2.1 Temperature	: -20°C to 60°C(-4° to 140°F)
5.2.2 Relative humidity	: 5% to 95%

6. Panel Characteristics

6.1 Type	: SDI V4
6.2 Size	: 42",932.94mm(W)X532.80mm(H) (W/Ostand)
6.3 Aspect ratio	: 16:9
6.4 Viewing angle	: Over 160°
6.5 Resolution	: 852X480
6.6 Weight	: 33.6kg ±0.5 kg (Net)w/o stand
6.7 Color	: 16.7 millions of colors (R/G/B each 256 scales)
6.8 Contrast	: Average 60:1 (In a bright room with 150Lux at center) Typical 10000:1 (In a dark room 1/100 White Window pattern at center).
6.9 Peak brightness	: Typical 1500cd/m² (1/25 White Window)

6.10 <u>Color Coordinate Uniformity</u>	: Contrast; Brightness and Color control at normal setting
Test Pattern	: Full white pattern



Average of point A,B,C,D and E +/- 0.01

6.11 Color temperature : Contrast at center (50); Brightness center (50); Colortemperature set at Natural
x=0.285±0.02
y=0.290±0.02

6.12 Cell Defect Specifications
Subject to Panel supplier specification as appends.

7. Front Panel Control Button

7.1 SEL. Up / Down Button	:	Select the Up/Down item in OSD menu.
VOL. Left/Right Button	:	Push the key to increase the volume left or right. When selecting the adjusting item in OSD menu increase or decrease the data-bar.
MENU Button	:	Display or Exit the OSD menu.
SOURCE Button	:	Press this button and use up/down button to select the signal sources. AV, S-Video, YPbPr 1,YPbPr 2, VGA or HDMI.
7.2 STANDBY Button	:	Switch on main power, or switch off to enter power Saving modes.
7.3 Main Power Switch	:	Turn on or off the unit.

8. OSD Function

8.1 Picture	:	Brightness; Contrast; Saturation; Peaking; Phase; Sharpness; Frequency; Picture Mode (Normal, Bright, Cinema, User); Color Temp (Warm, Normal, Cool); etc.
8.2 Window	:	Image Size (Fill All, Force 4:3, Letter Box, Wide, Anamorphic, etc); H Position; V Position; H Resolution; Freeze Window (Off, On)
8.3 Audio	:	Balance; Audio Mode (BBE, Cinema, Music, News, User) Speaker (Internal, External); AVC (Off, On) Equalizer (120Hz, 500Hz, 1.2kHz, 3kHz, 12kHz)
8.4 Options	:	Osd Timeout (5 Sec, 15 Sec, 60 Sec); Menu Background (Opaque, Translucent); Language(English, French, Spanish); Default Setting; Close Caption Mode; Close Caption; Content Blocking; Timer
8.5 Layout	:	Full Screen; PIP; Split Screen

9. Agency Approvals

Safety : UL, FCC, FDA
 Emissions : UL, FCC, FDA

10. Reliability

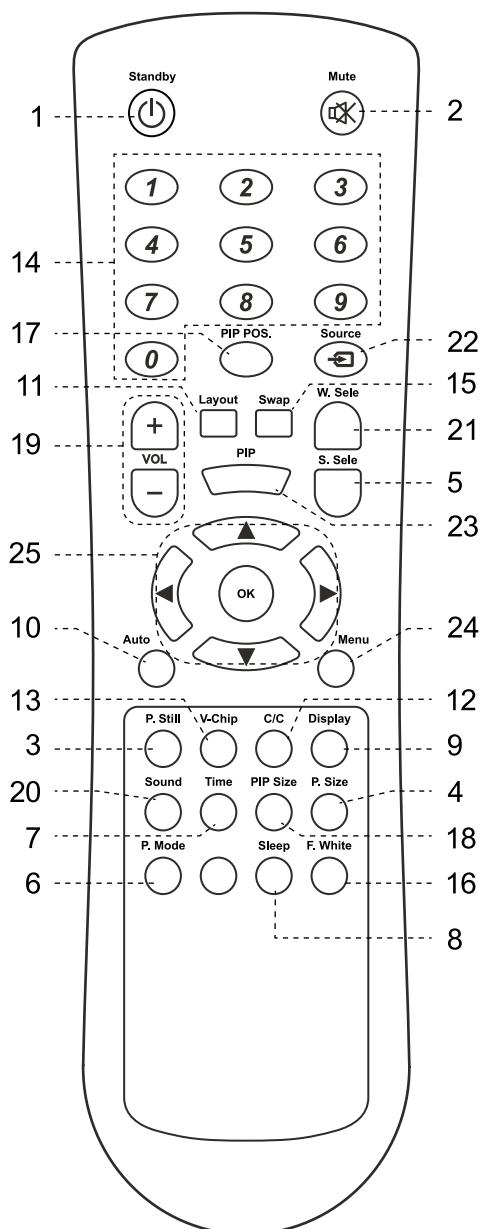
MTBF : 20,000 hours (Use moving picture signal at 25°C ambient)

11. Accessories

User manual x1, Remote control x1, Stand x 1, Battery x 2, AC Cable x 1

12. Remote Control

- 1 **Standby(∅)**: Press this button to turn off to standby and turn on from standby.
- 2 **Mute(🔇)**: Press this button to quiet the sound system. Press again to reactivate the sound system.
- 3 **P. Still**: Press this button to hold on the screen. Press again to normal.
- 4 **P. Size**: When the input source is YPbPr 1, YPbPr 2, VGA or HDMI, press this button, the picture will change according to Fill All, Force 4:3, Letter Box, Wide or Anamorphic. When the input source is AV or S-Video, press this button, the picture will change according to Fill All, 4:3, Letter Box, Wide or Anamorphic.
- 5 **S. Sele**: Press this button to select the sound output from Main Window or Sub Window.
- 6 **P. Mode** : Press the button to select different picture effect.
- 7 **Time**: Press this button to pop up the "Clock Set" menu.
- 8 **Sleep**: Press this button to select the sleep time.
- 9 **Display**: Press the button to display the source information.
- 10 **Auto**: The Display automatically adjusts the phase, vertical / horizontal position when pressing this button in VGA mode.
- 11 **Layout**: Press this button to pop up Layout menu.
- 12 **C/C**: Press this button to enter the Closed Caption Function. (Only for AV or S-Video)



(Continued on next page)

13 V-Chip: Press this button to enter the V-Chip Function. (Only for AV or S-Video)

14 Number buttons: Use these buttons to enter the password.

15 Swap: Press this button to switch the Main window or Sub window pictures in PIP and Split Screen.

16 F. White: Press this button to show a full white picture.

17 PIP POS. : Press the button to select different Image Position in PIP Mode.

18 PIP Size : Press the button to select different Image Size in PIP Mode.

19 VOL +/- : Press these buttons to increase or decrease the volume.

20 Sound: Press the button to select different sound effect.

21 W. Sele: Press this button to select the Main Window or Sub Window.

22 Source: Press this button and use \blacktriangle / \blacktriangledown button to select the signal sources. AV, S-Video, YPbPr 1, YPbPr 2, VGA or HDMI.

23 PIP: Press this button to change different Picture Mode.

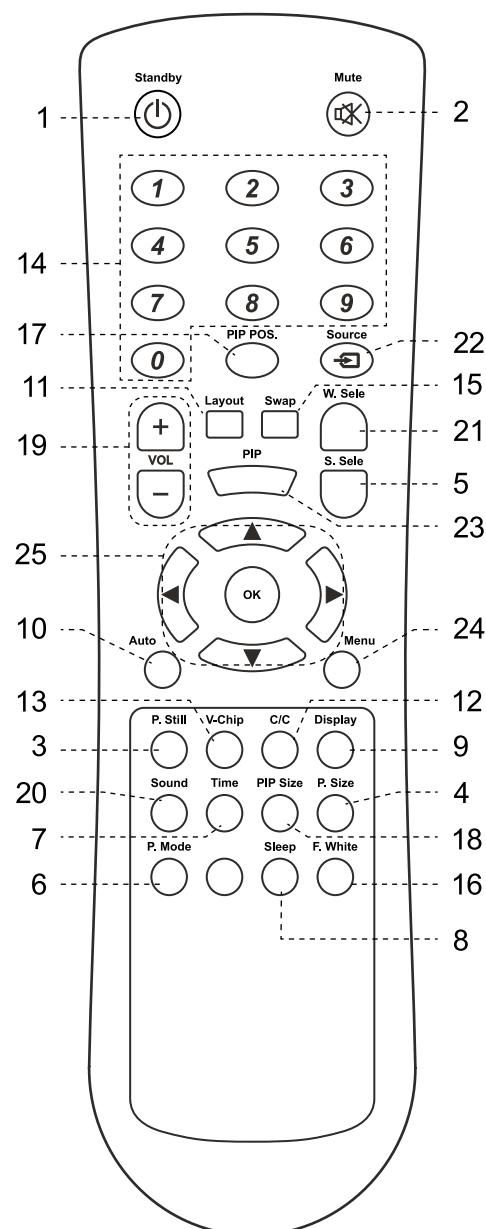
24 Menu: Press this button to pop up the OSD Menu and press it again to exit the OSD Menu.

25 OK : Press to enter or confirm.

\blacktriangleleft / \triangleright : They are used as \blacktriangleleft / \triangleright buttons in the OSD Menu screen.

\blacktriangle / \blacktriangledown : They are used as \blacktriangle / \blacktriangledown buttons in the OSD Menu screen.

They also can be used for the selection of the program when the OSD Menu is not shown on the screen, but only for the Model with Tuner.



13. Support the Signal Mode

13.1. VGA Mode, HDMI Mode or HDTV Mode (YPbPr 1 or YPbPr 2)

Mode	Resolution	Horizontal Frequency (kHz)	Vertical Frequency (Hz)	Dot Clock Frequency (MHz)
VGA Mode	640 x 480	31.50	60.00	25.18
	800 x 600	37.90	60.32	40.00
	1024 x 768	48.40	60.00	65.00
	1280 x 1024	64.00	60.01	108.00
HDMI Mode	1080i	33.75	60.00	74.25
	720p	45.00	60.00	74.25
	480p	31.468	59.94	27.00
HDTV Mode (YPbPr1/YPbPr2)	1080i	33.75	60.00	74.25
	720p	45.00	60.00	74.25
	480p	31.468	59.94	27.00
	480i	15.734	59.94	13.50

13.2.PIP/PBP Screen Mode

Items		VGA (Max.)	HDMI/YPbPr1/YPbPr2		
			480p	720p	1080i
PIP	Main	1024 x 768	OK	OK	OK
	Sub	Large	OK	OK	OK
		Middle	OK	OK	X
		Small	OK	OK	X
PBP	Main	1024 x 768	OK	OK	OK
	Sub	1024 x 768	OK	OK	OK

Note:

- “X” means out of range (can not show).
- When the signal received by the Display exceeds the allowed range, a warning message shall appear on the screen.
- You can confirm the input signal format from the on-screen.
- VGA 1280 x 1024 Mode don't recommend working in PIP/PBP Screen Mode.

PHYSICAL CHARACTERISTICS

14. Power Cord

Length : 1.8m nominal

Type : optional

15. Cabinet

15.1 Color : black colour as defined by colour plaque reference number

15.2 Weight(W/O stand)

Net weight : 33.6kg

15.3 Dimensions (W/O stand&speaker)

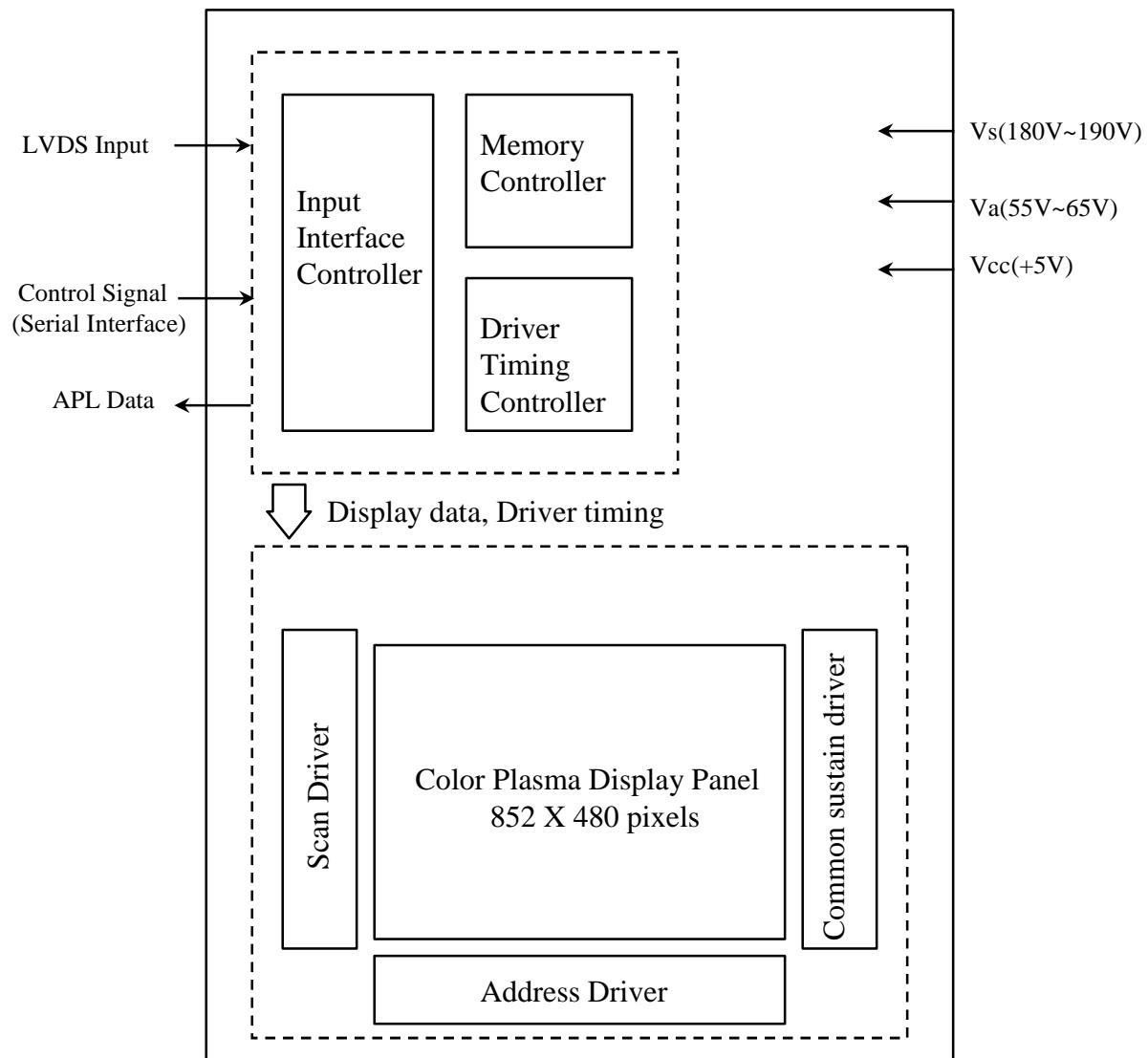
Width : 1050mm

Height : 657mm

Depth : 99.5mm

Block Diagram

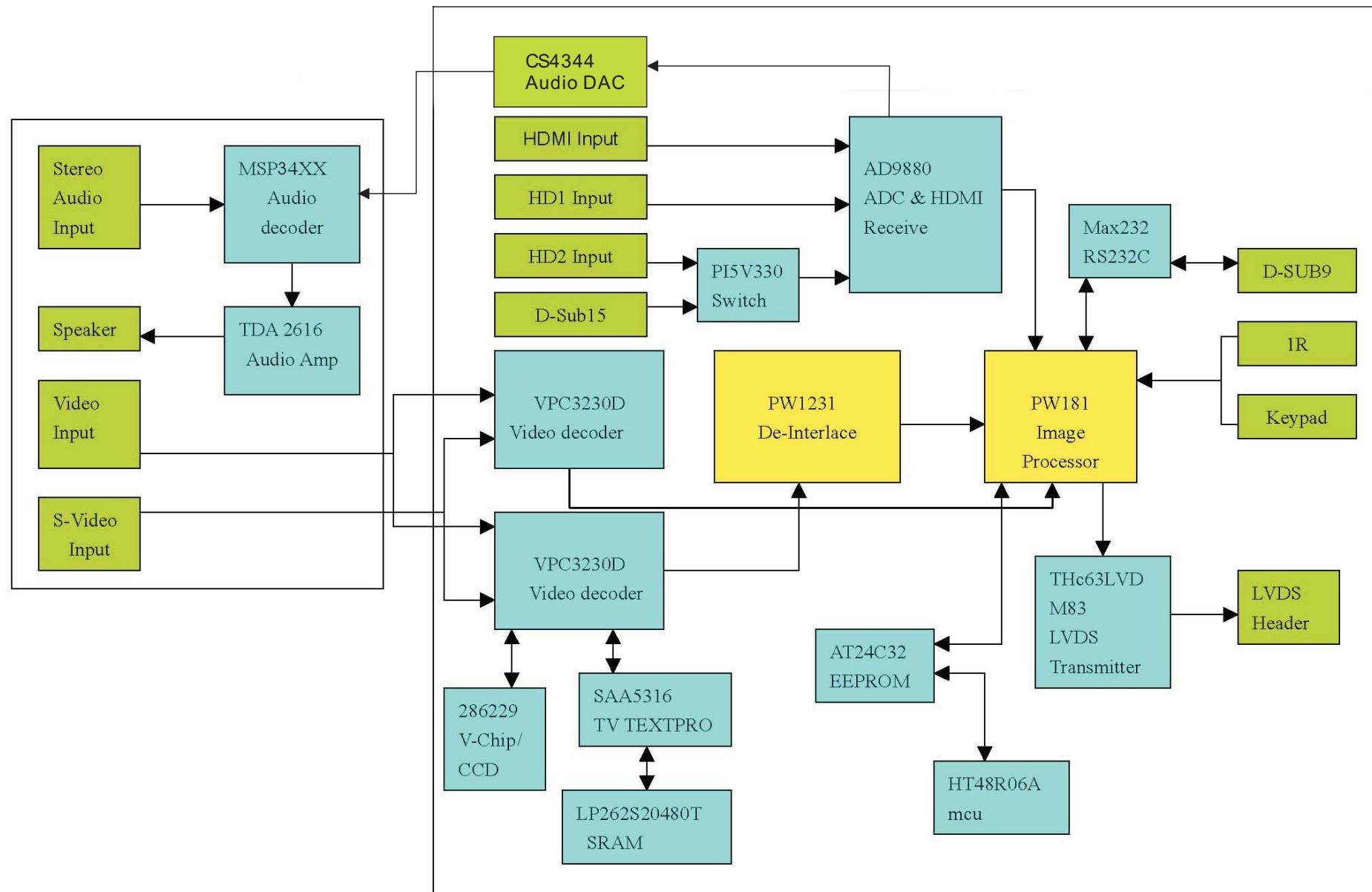
Product Specification of PDP Module



Applied Voltage level is specified at the time when Full-White pattern is displayed on the panel.

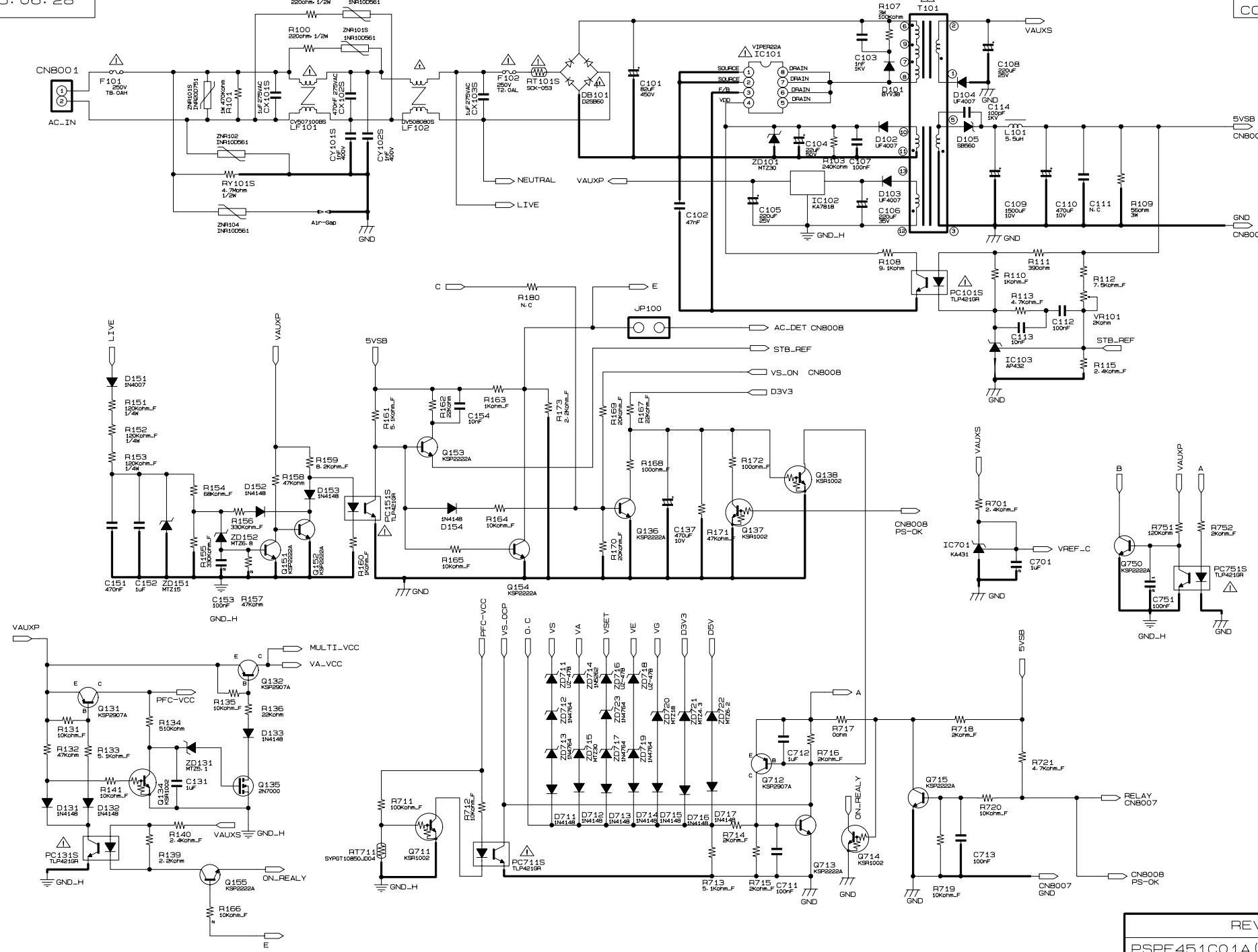
Block Diagram

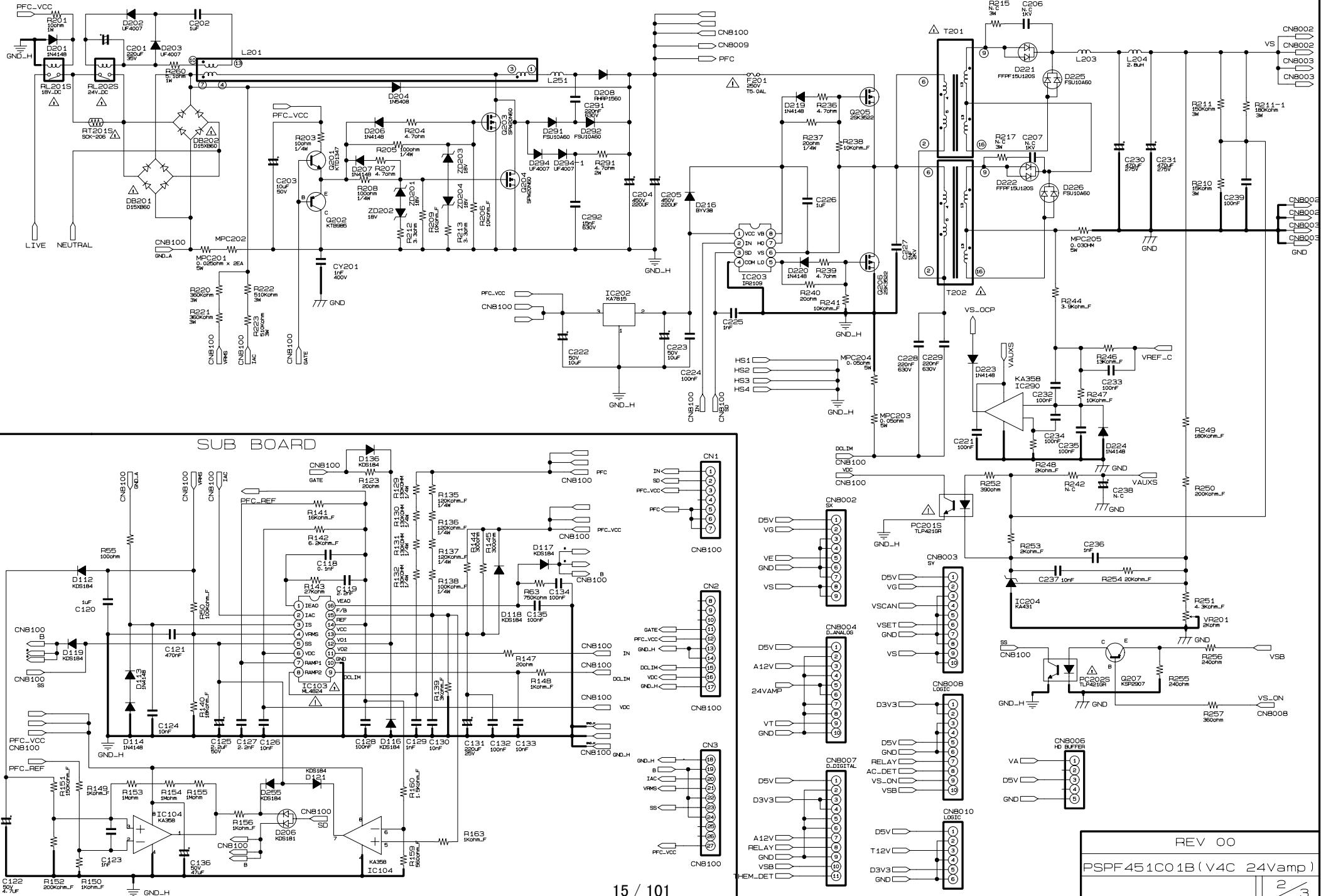
MAIN/AUDIO BOARD

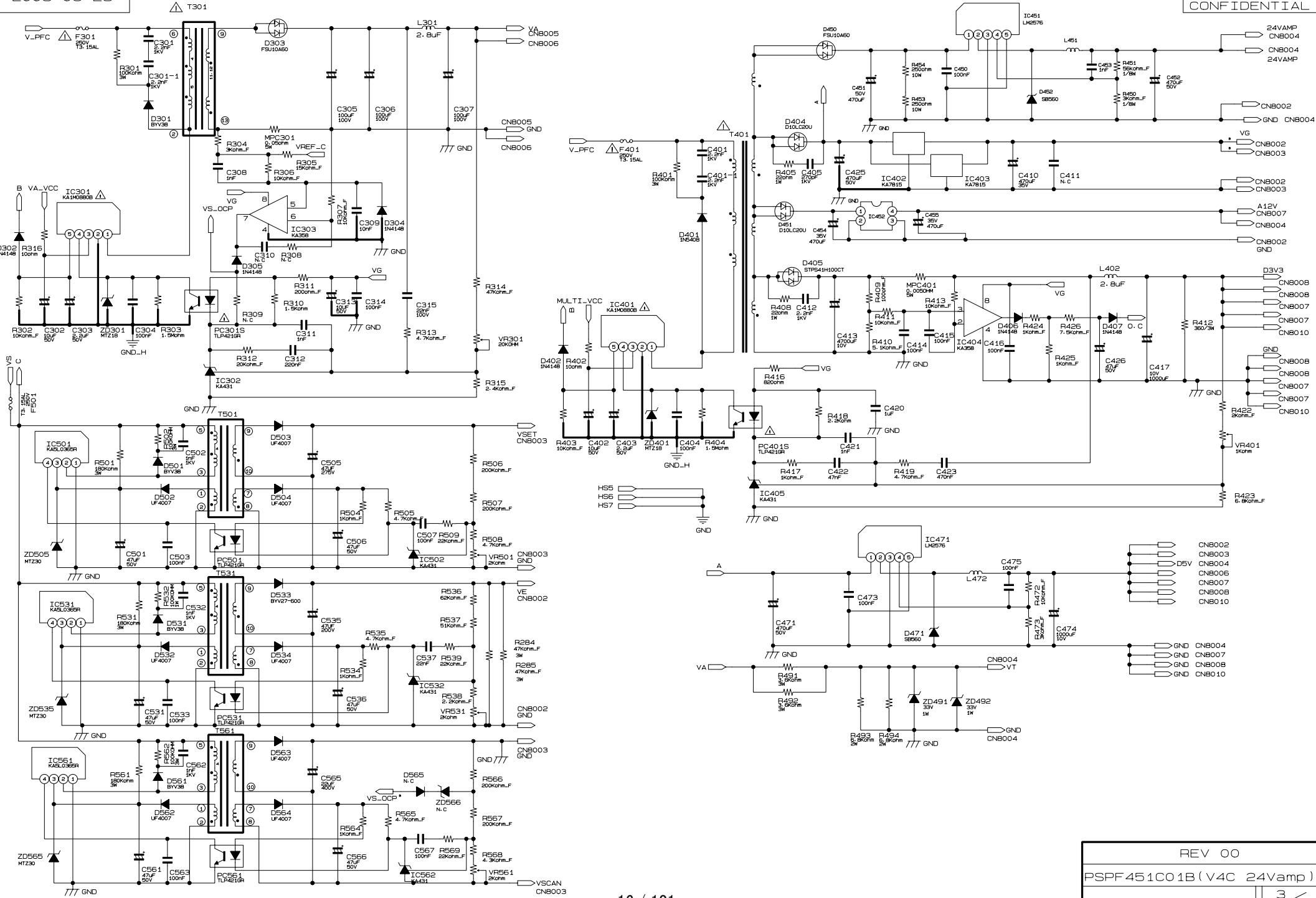


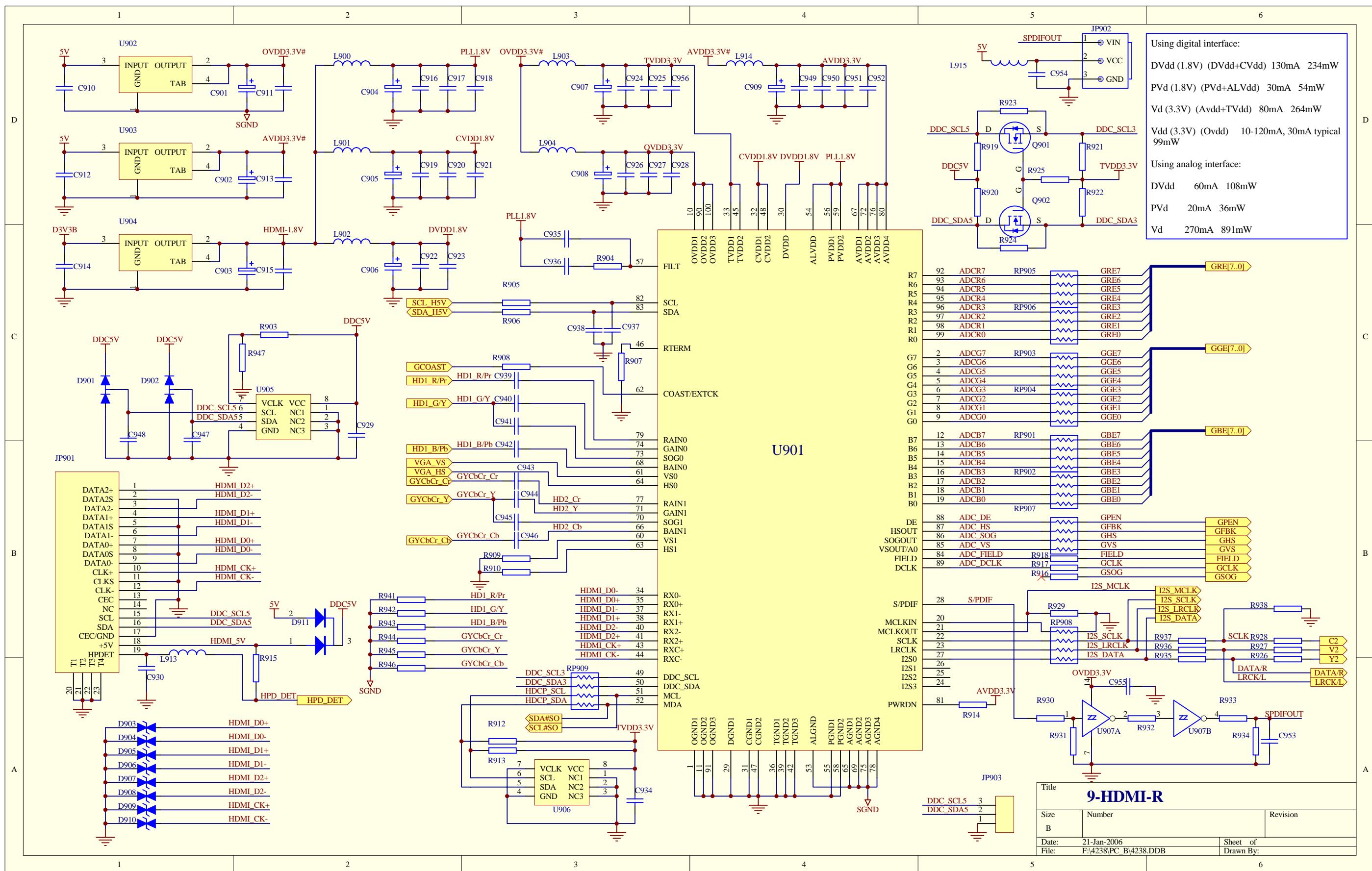
Circuit Diagram

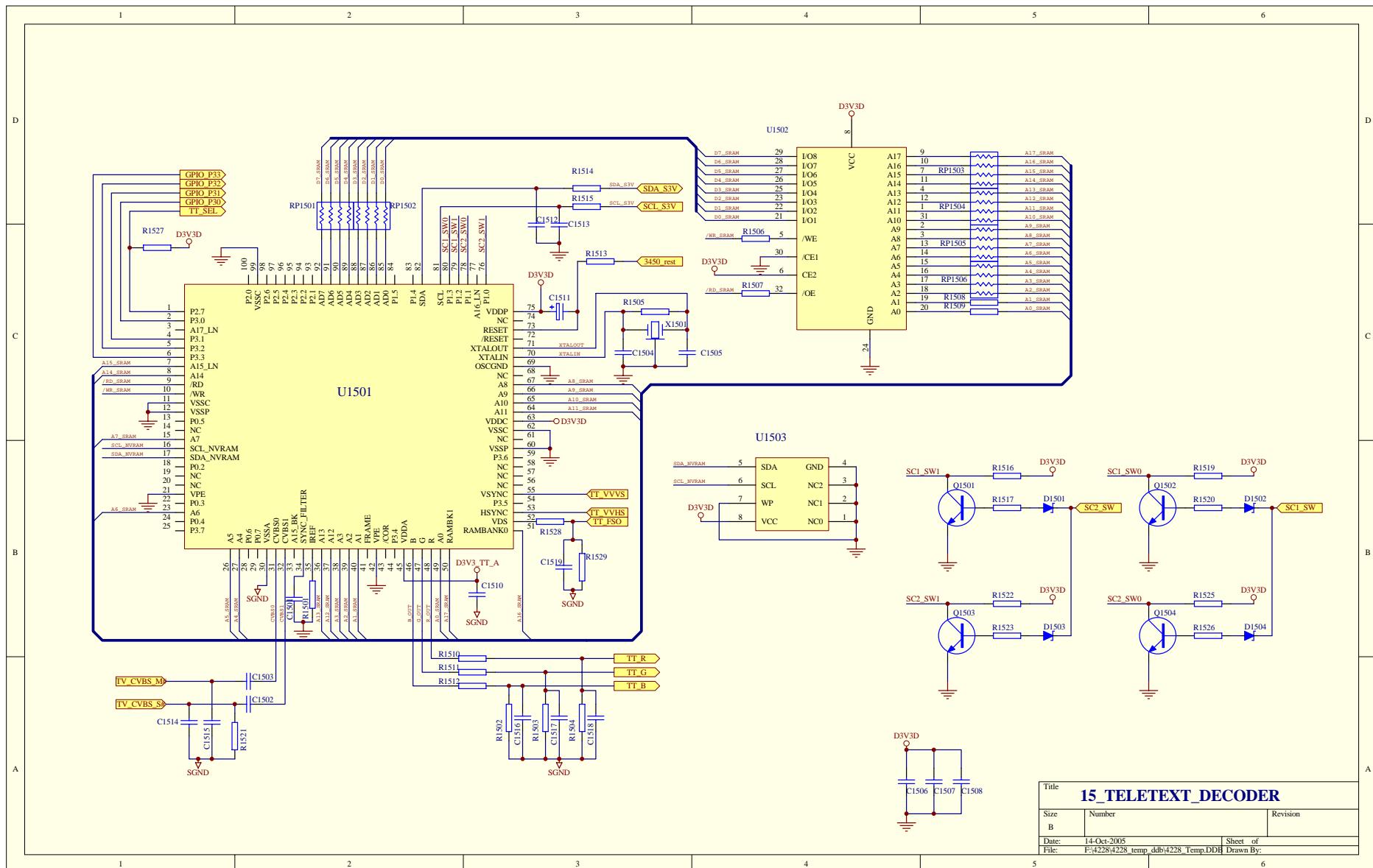
- Power supply board of Audio Amplifier, MPT012A
- Main (Video) board
- Audio/Tuner board
- Keypad board
- Remote control receiver board
- Remote control board

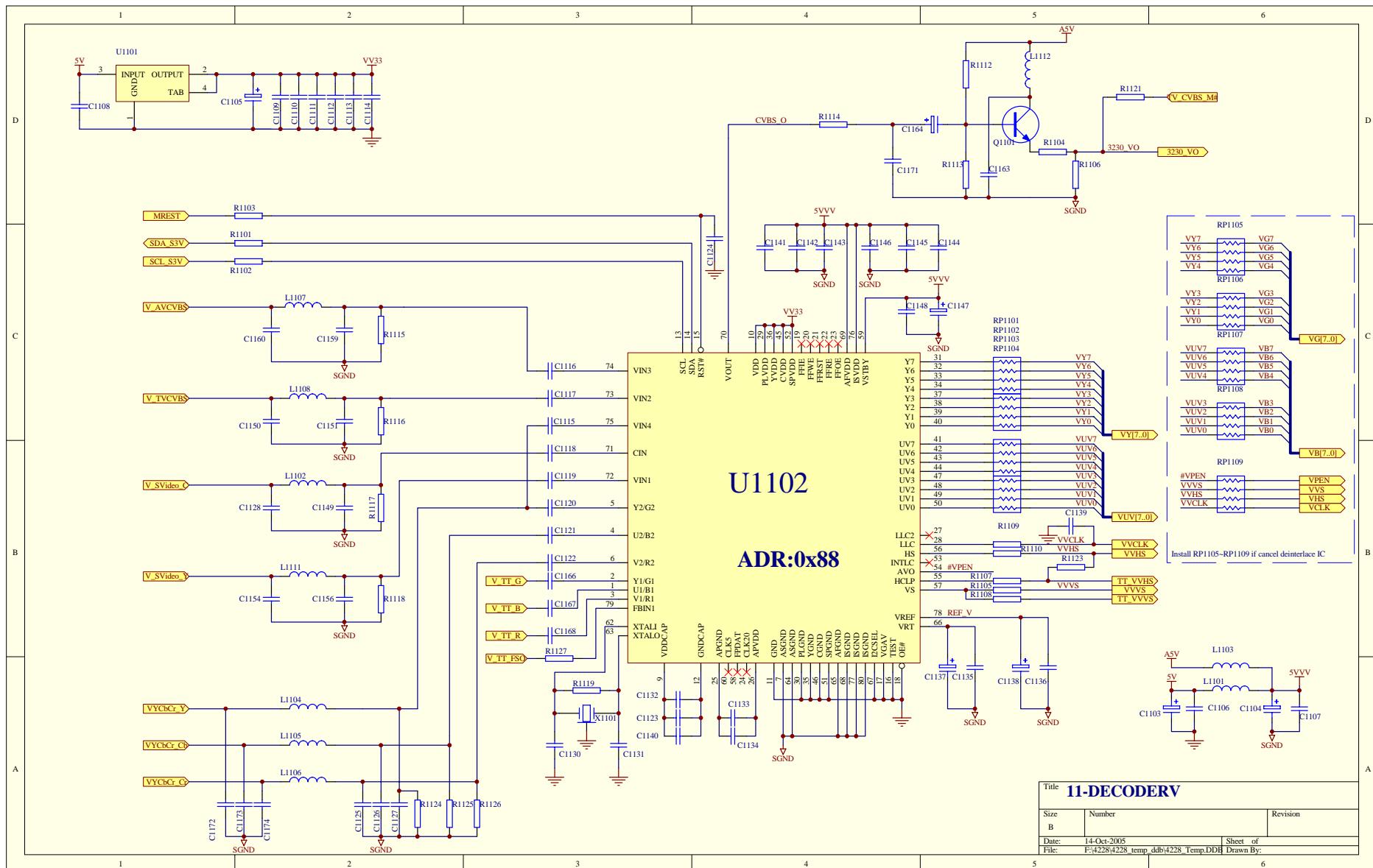


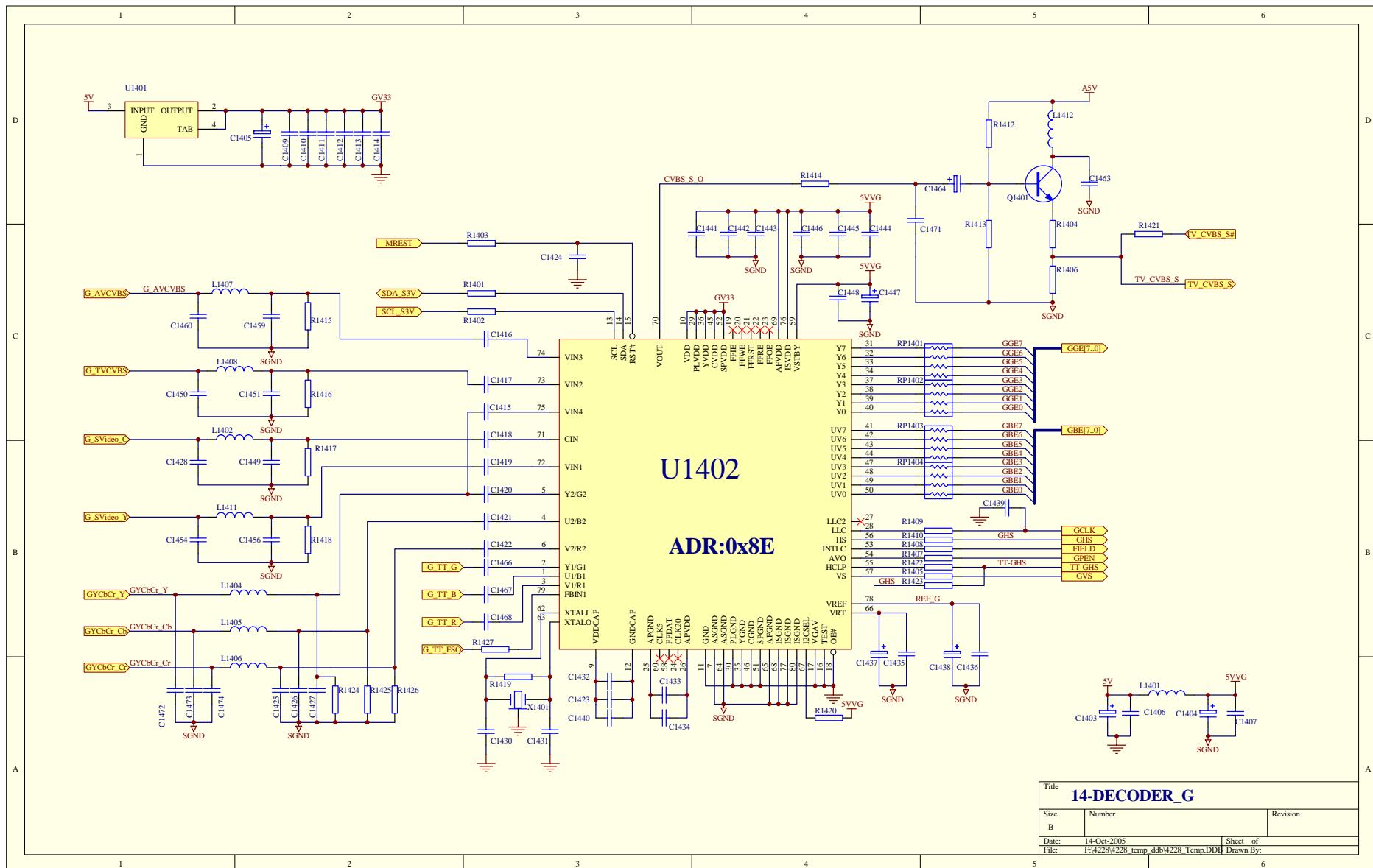


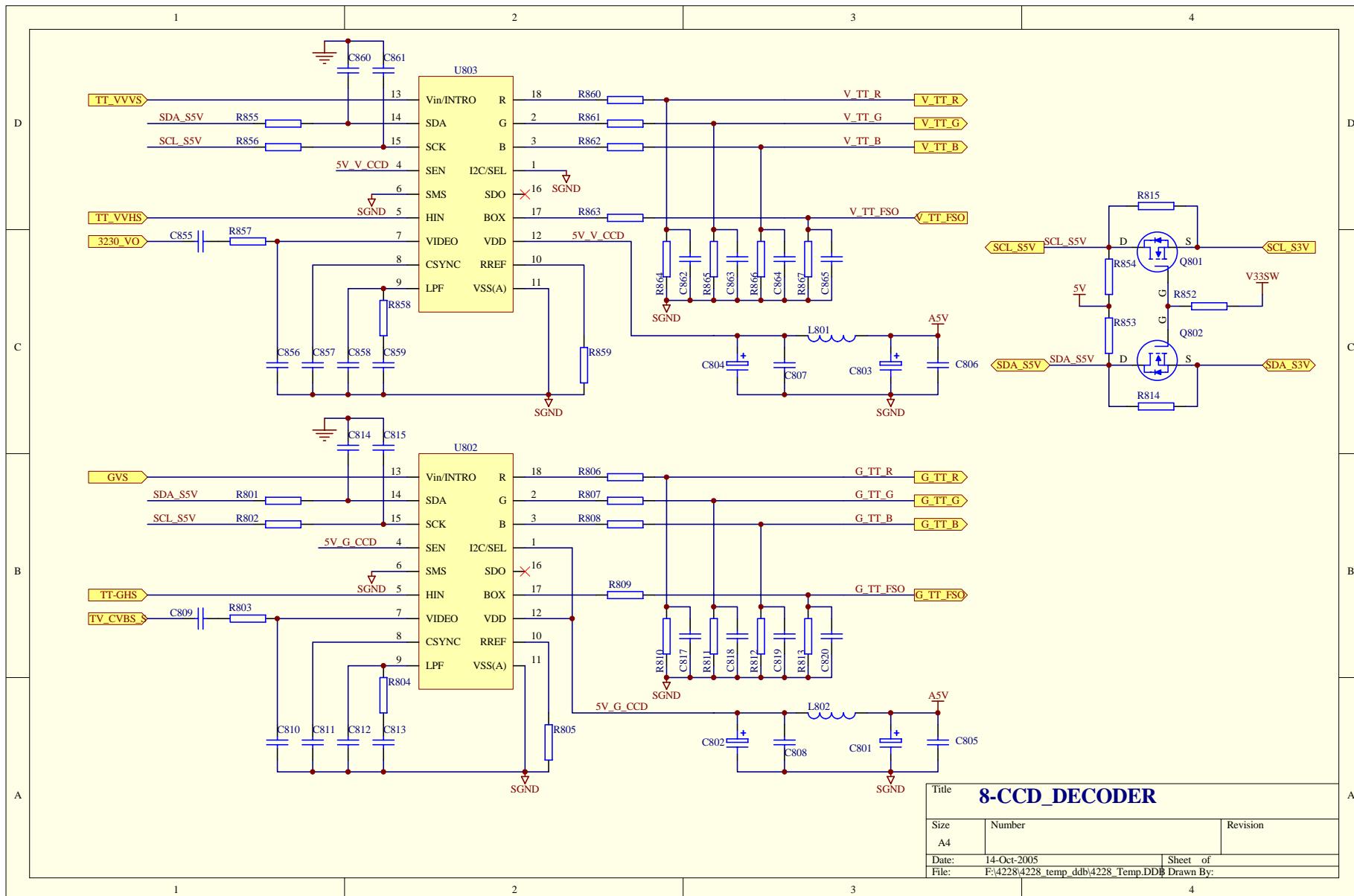


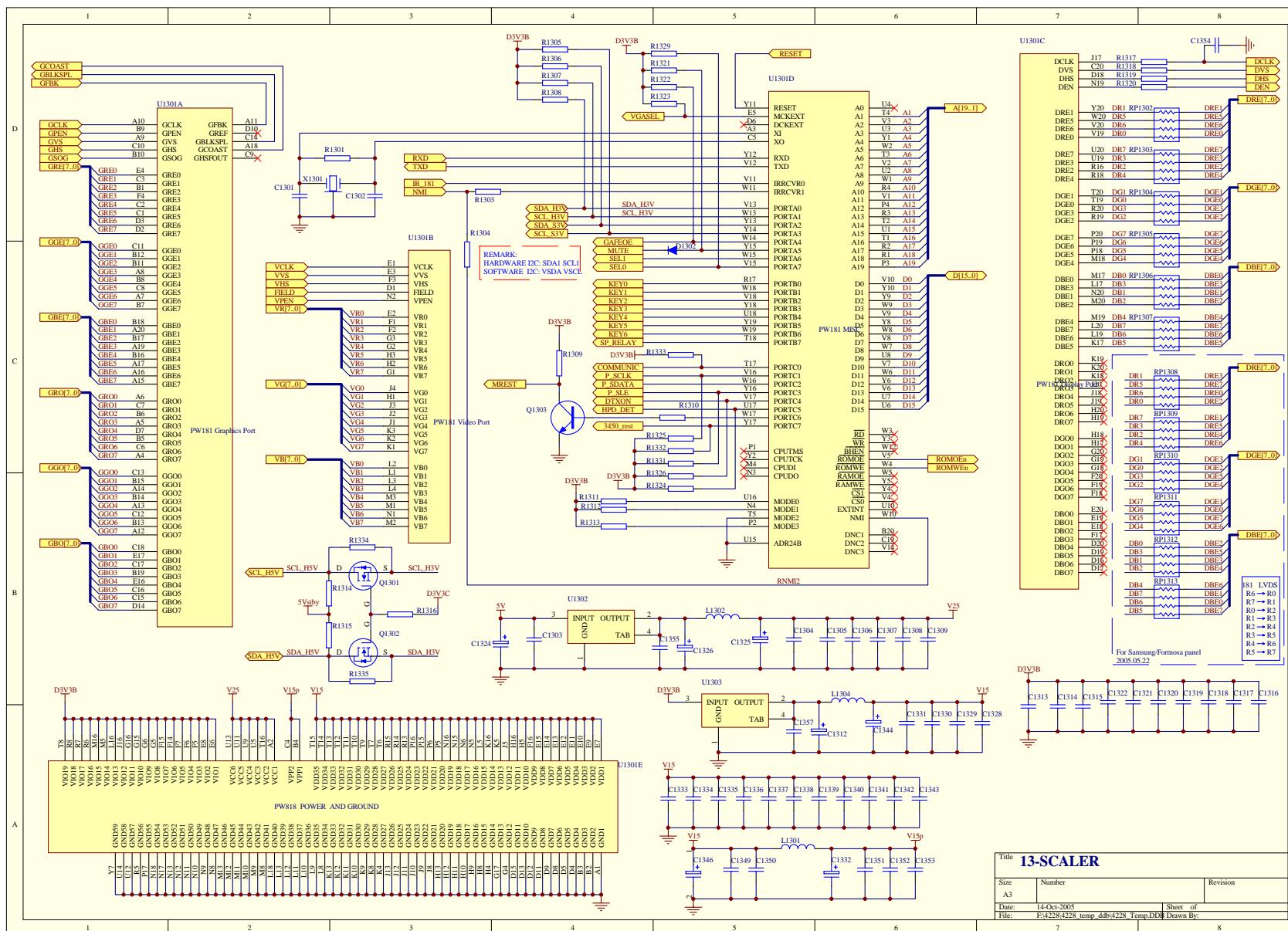


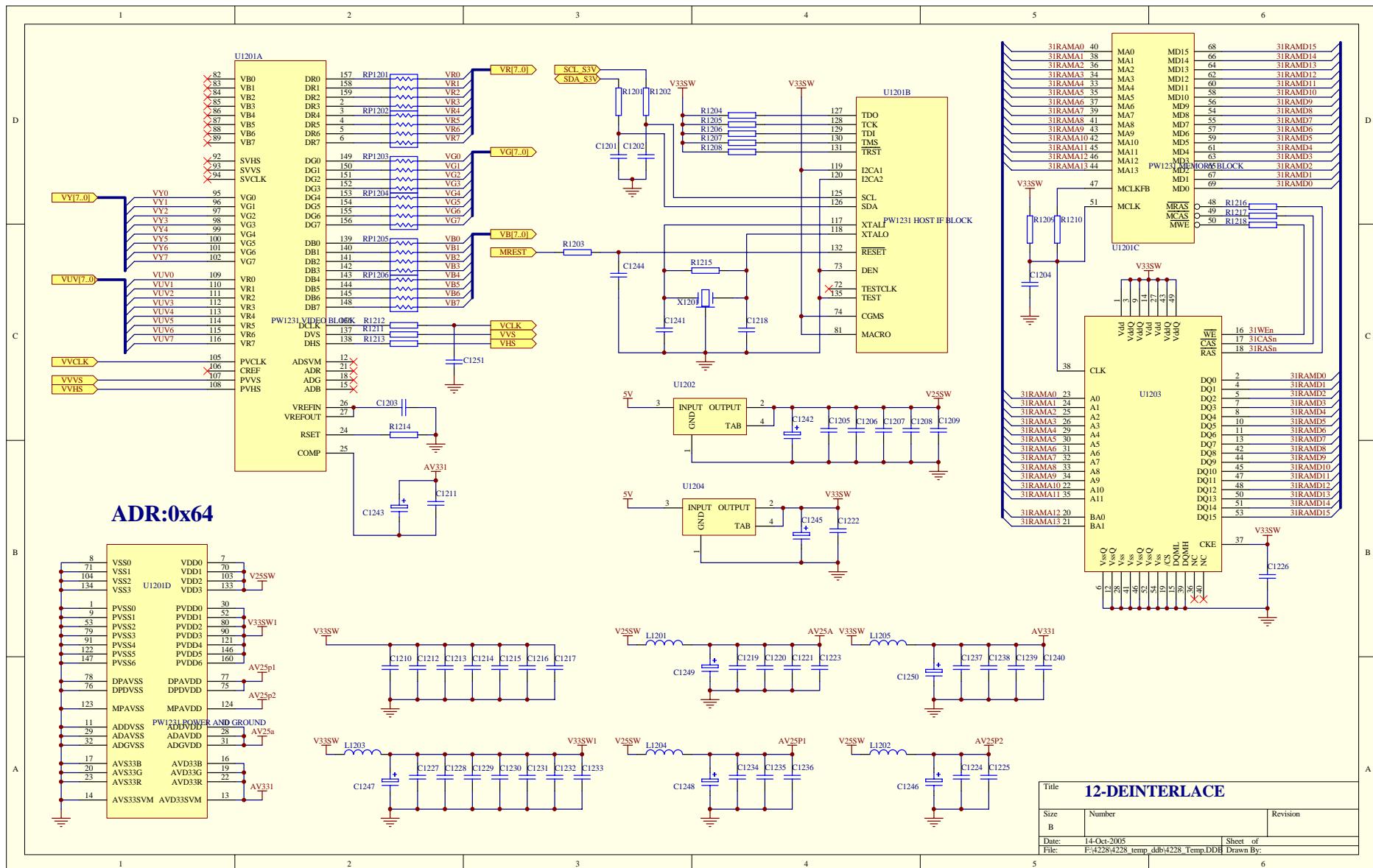


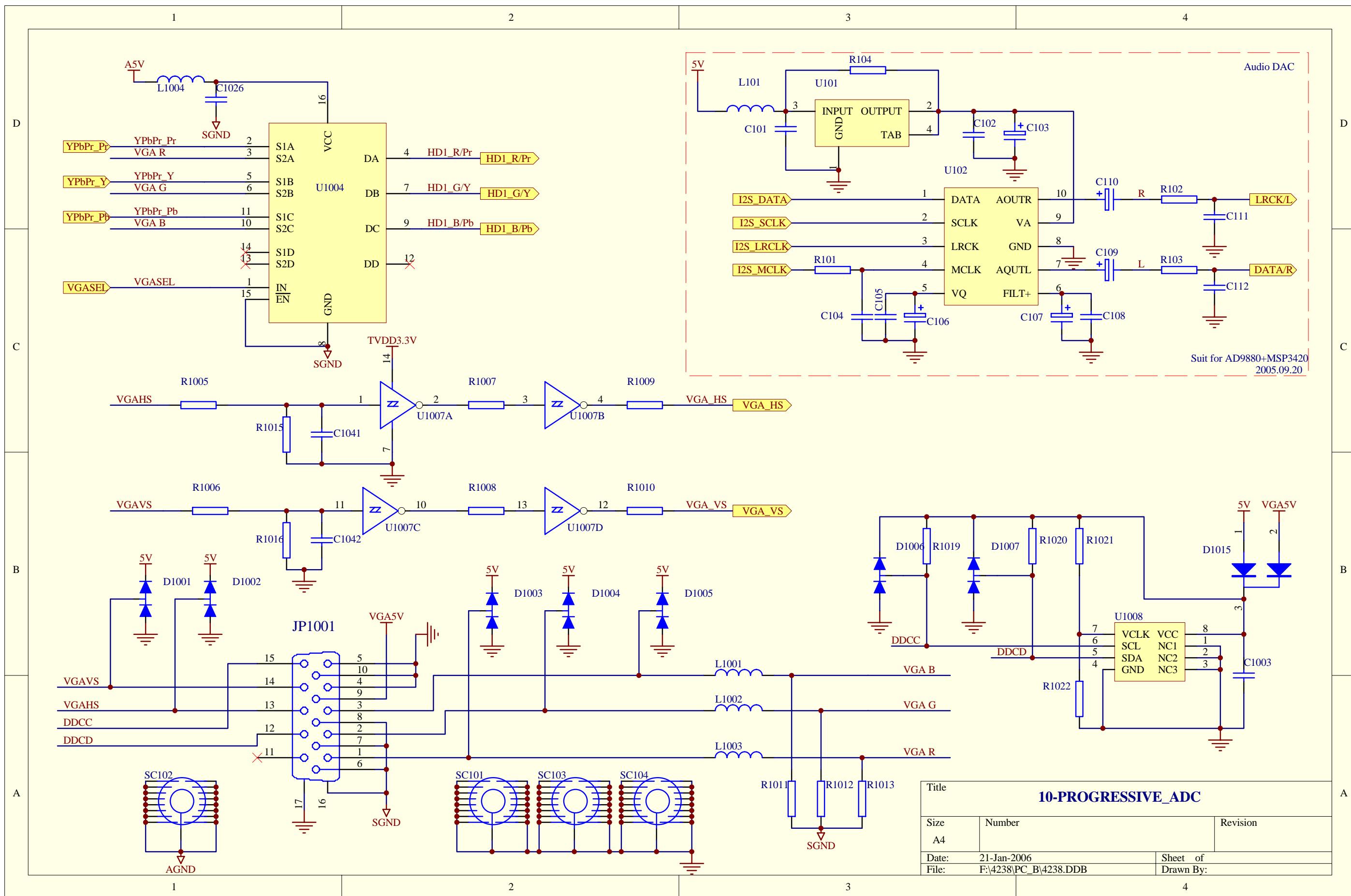


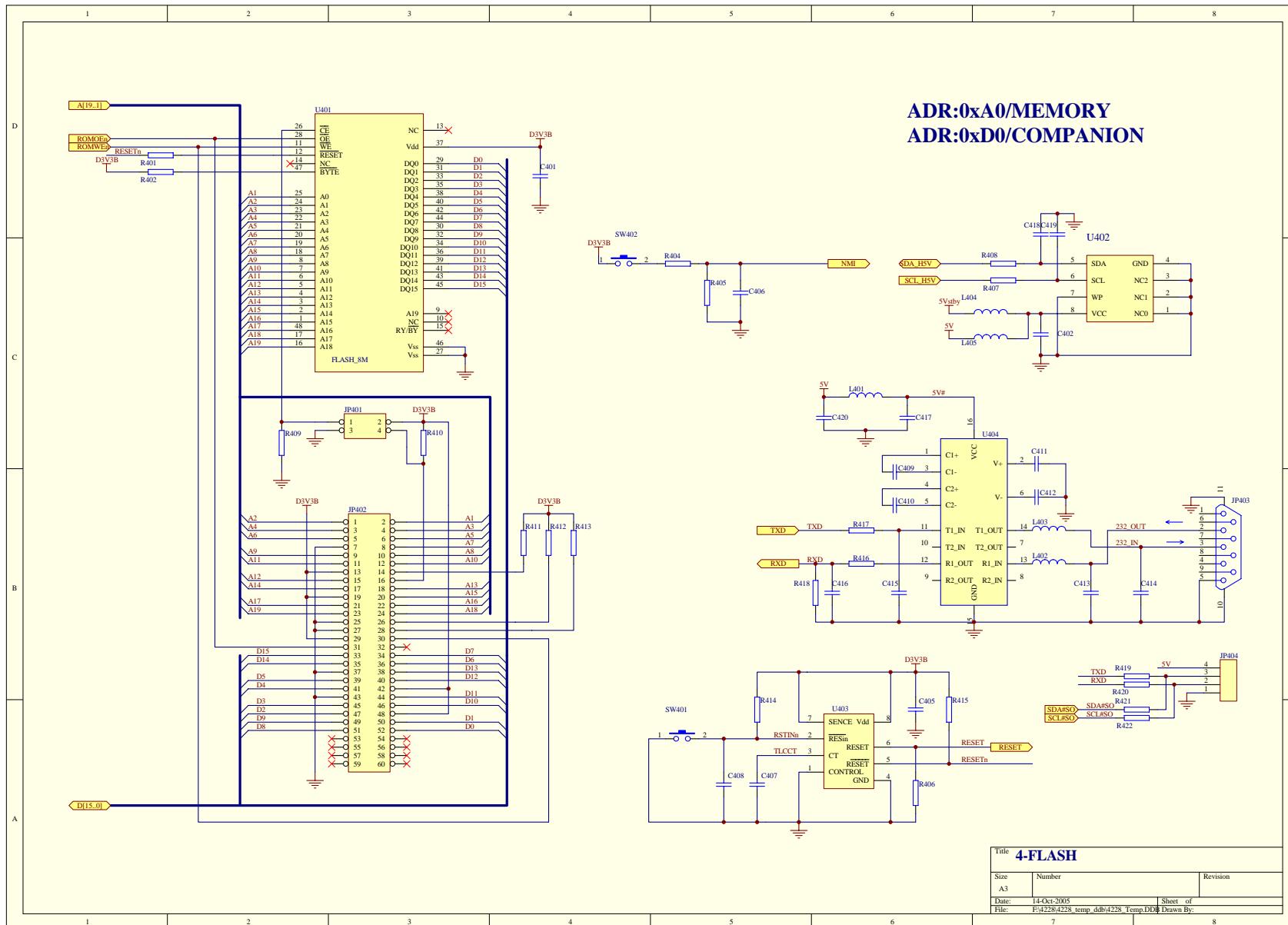


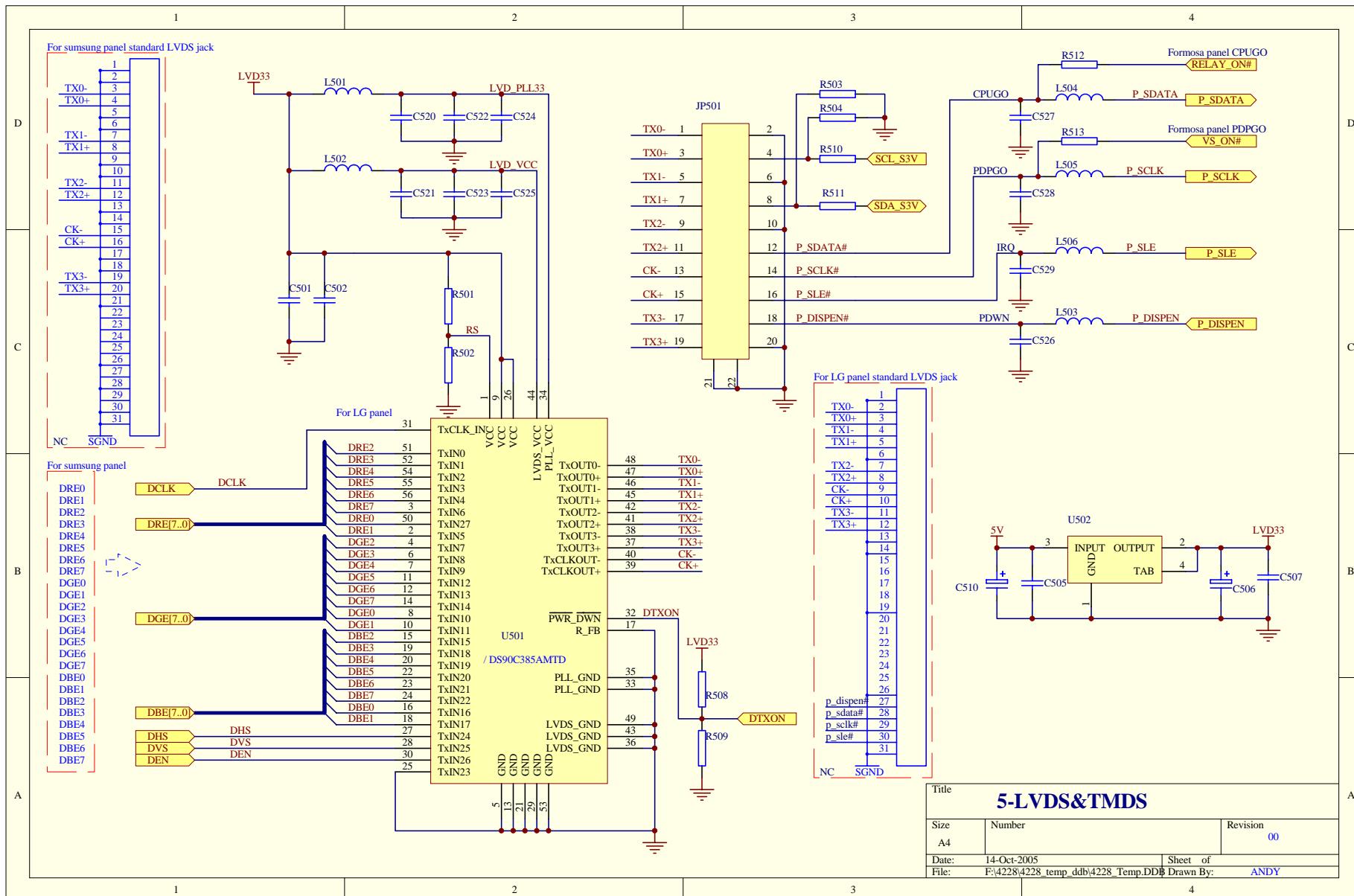


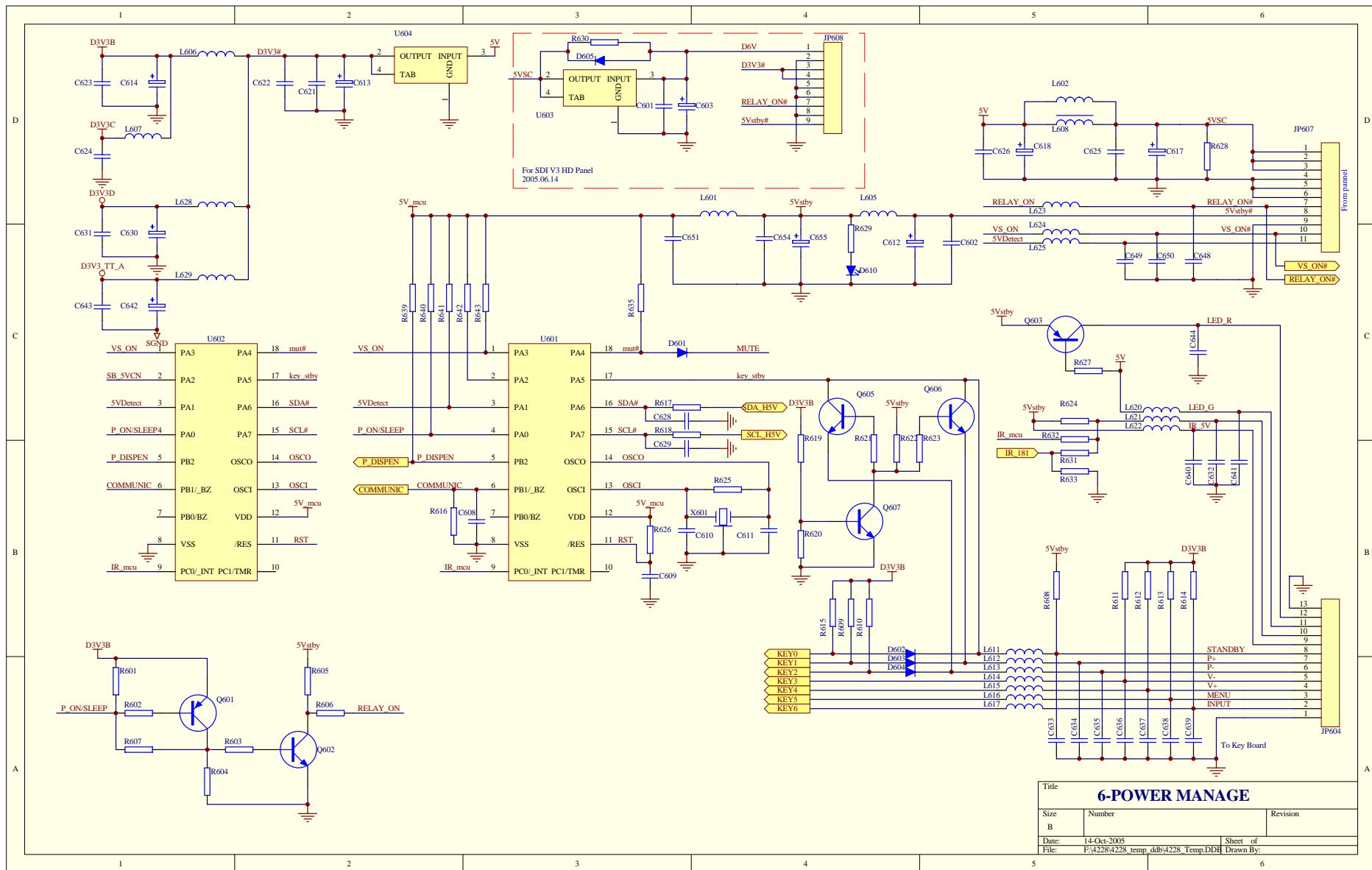


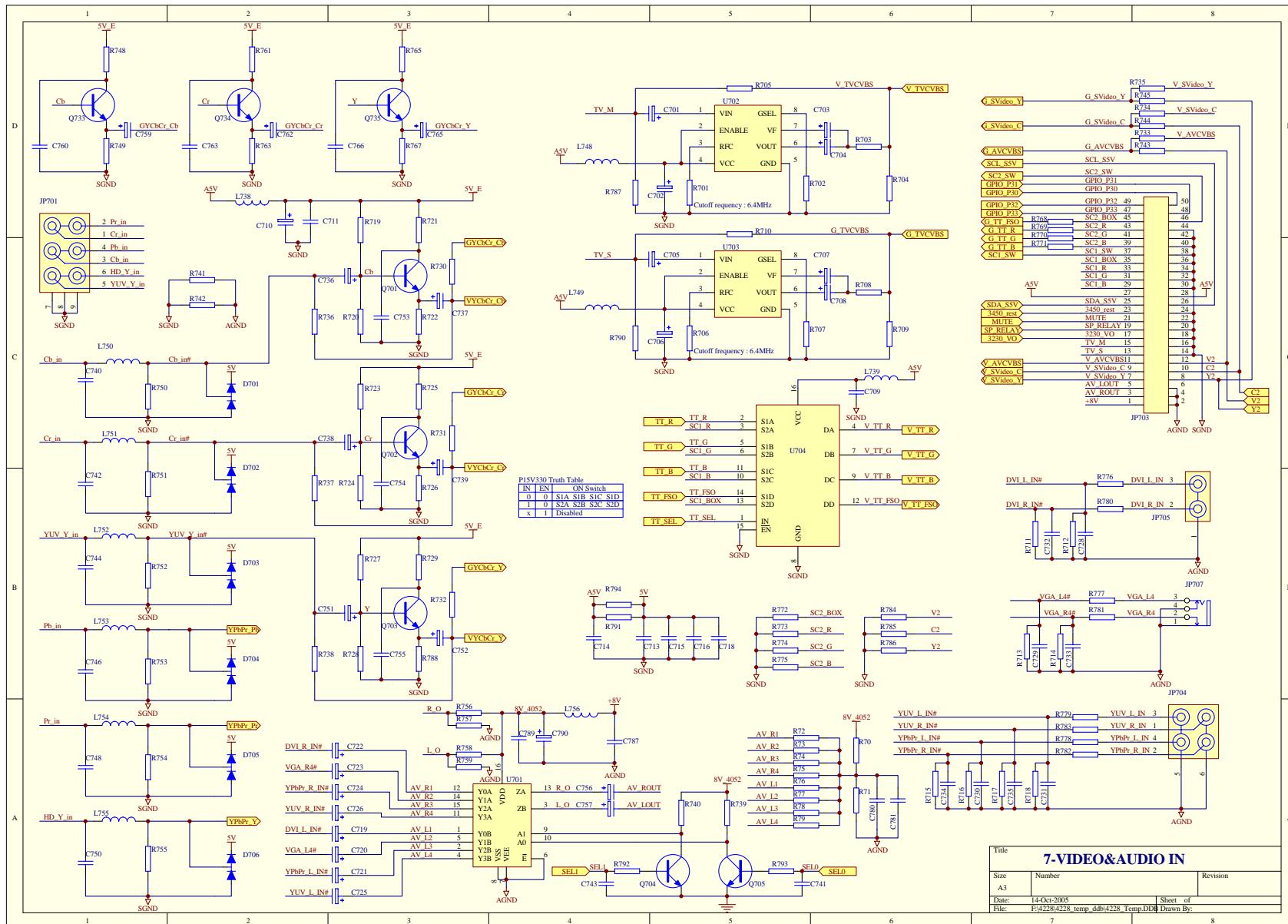


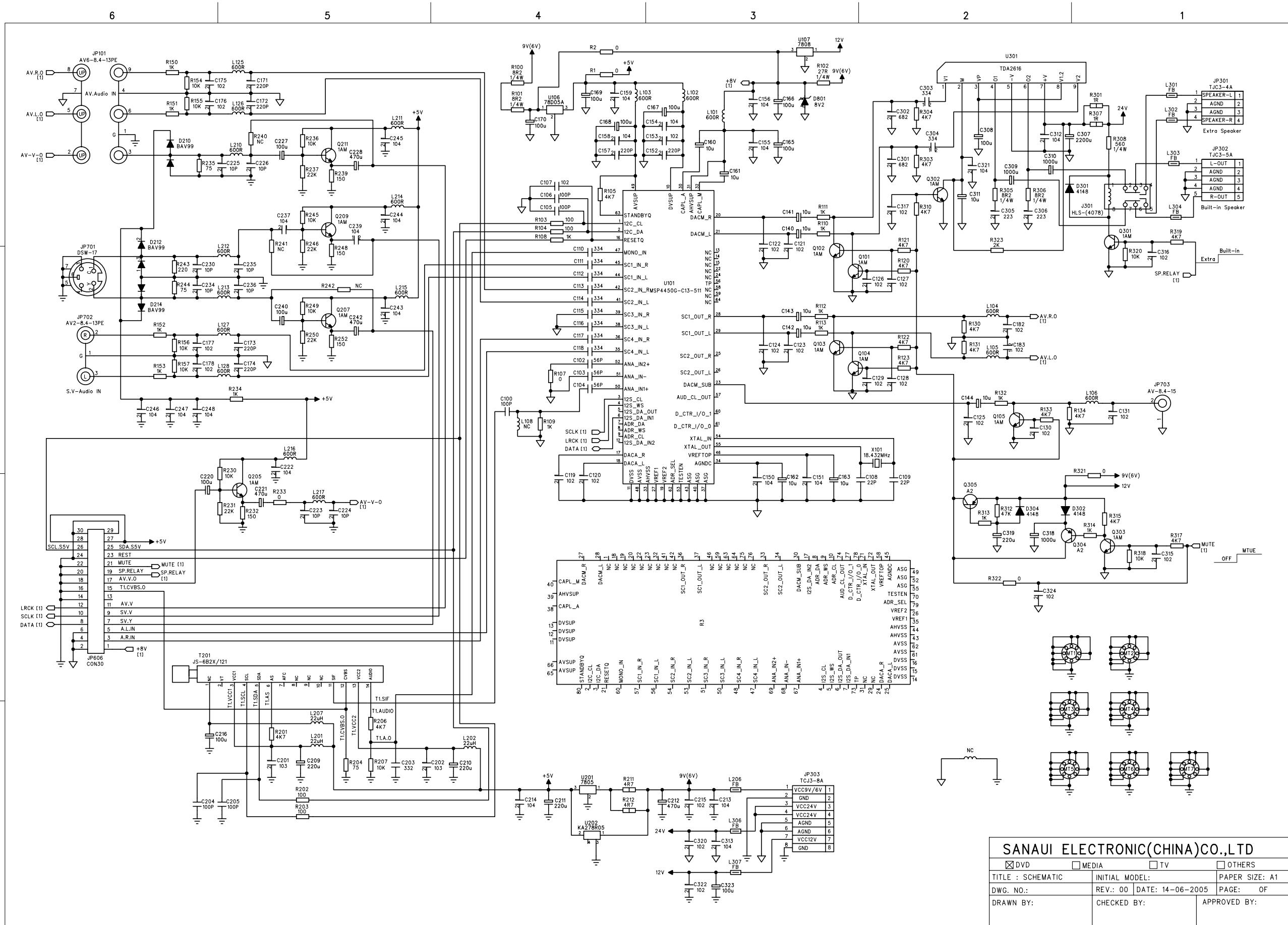












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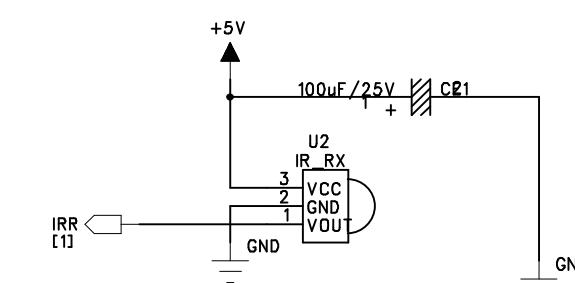
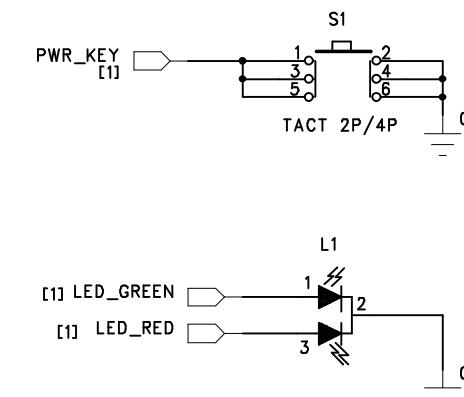
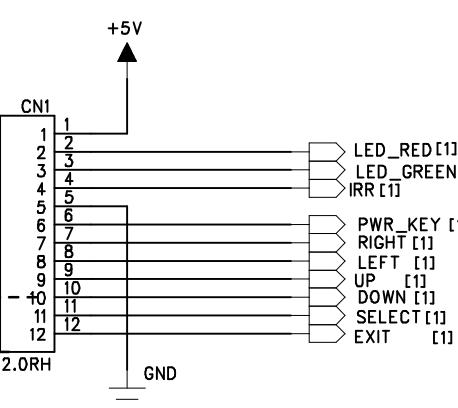
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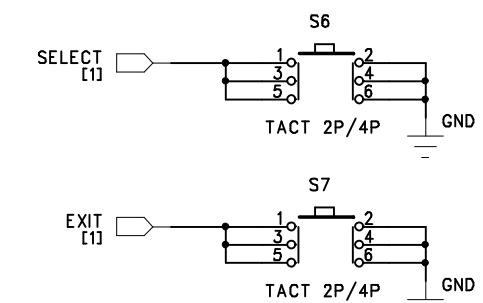
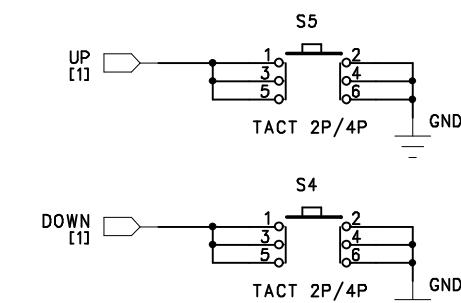
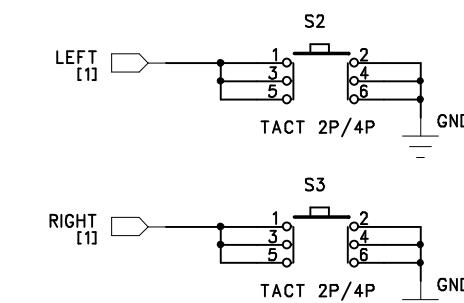
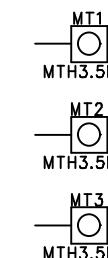
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6

DUBHE OSD
6-Key OSD



OSD I/F Connector



	Project:		Rev:
	Project Name		1.2
	Title:		
	DUBHE OSD		

Date: June. 15, 2004

Sheet: xx of xx

1

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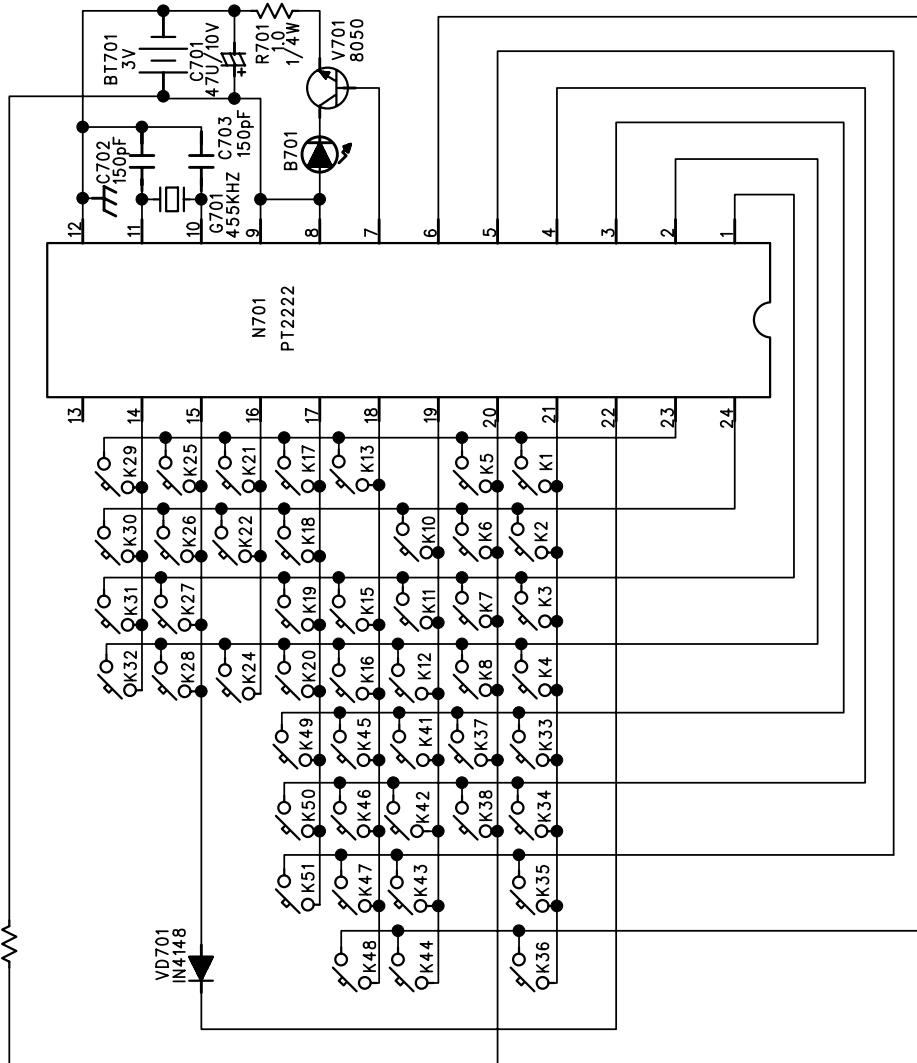
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REMOTE PCB

R702
56K

REMOTE CONTROL CODE ASSIGNMENT

KEY NO.	KEY NAME	DATA CODE	KEY NO.	KEY NAME	DATA CODE
K1	POWER	00	K33	dumb	40
K2	1	01	K34	dumb	41
K3	2	02	K35	dumb	42
K4	3	03	K36	dumb	43
K5	P.MODE	04	K37	MUTE	44
K6	4	05	K38	INFO	45
K7	5	06	K39	nil	46
K8	6	07	K40	nil	47
K9	nil	08	K41	100	48
K10	7	09	K42	PREV	49
K11	8	0A	K43	P.STILL	4A
K12	9	0B	K44	SOUND	4B
K13	MTS	0C	K45	SLEEP	4C
K14	nil	0D	K46	TIME	4D
K15	S.SELECT	0E	K47	Picture	4E
K16	OK	0F	K48	CH.Erase	4F
K17	CH.+	10	K49	CH.Save	50
K18	Vol.+	11	K50	C/C	51
K19	Vol.-	12	K51	V-CH/P	52
K20	CH.-	13	K52	nil	53
K21	MENU	14	K53	nil	54
K22	Source	15	K54	nil	55
K23	nil	16	K55	nil	56
K24	P.SIZE	17	K56	nil	57
K25	0	18	K57	nil	58
K26	F.White	19	K58	nil	59
K27	PIP Source	1A	K59	nil	5A
K28	EXIT	1B	K60	nil	5B
K29	PIP	1C	K61	nil	5C
K30	SWAP	1D	K62	nil	5D
K31	PIP CH-	1E	K63	nil	5E
K32	PIP CH+	1F	K64	nil	5F

CUSTOM CODE: 20DD

FOR NTSC

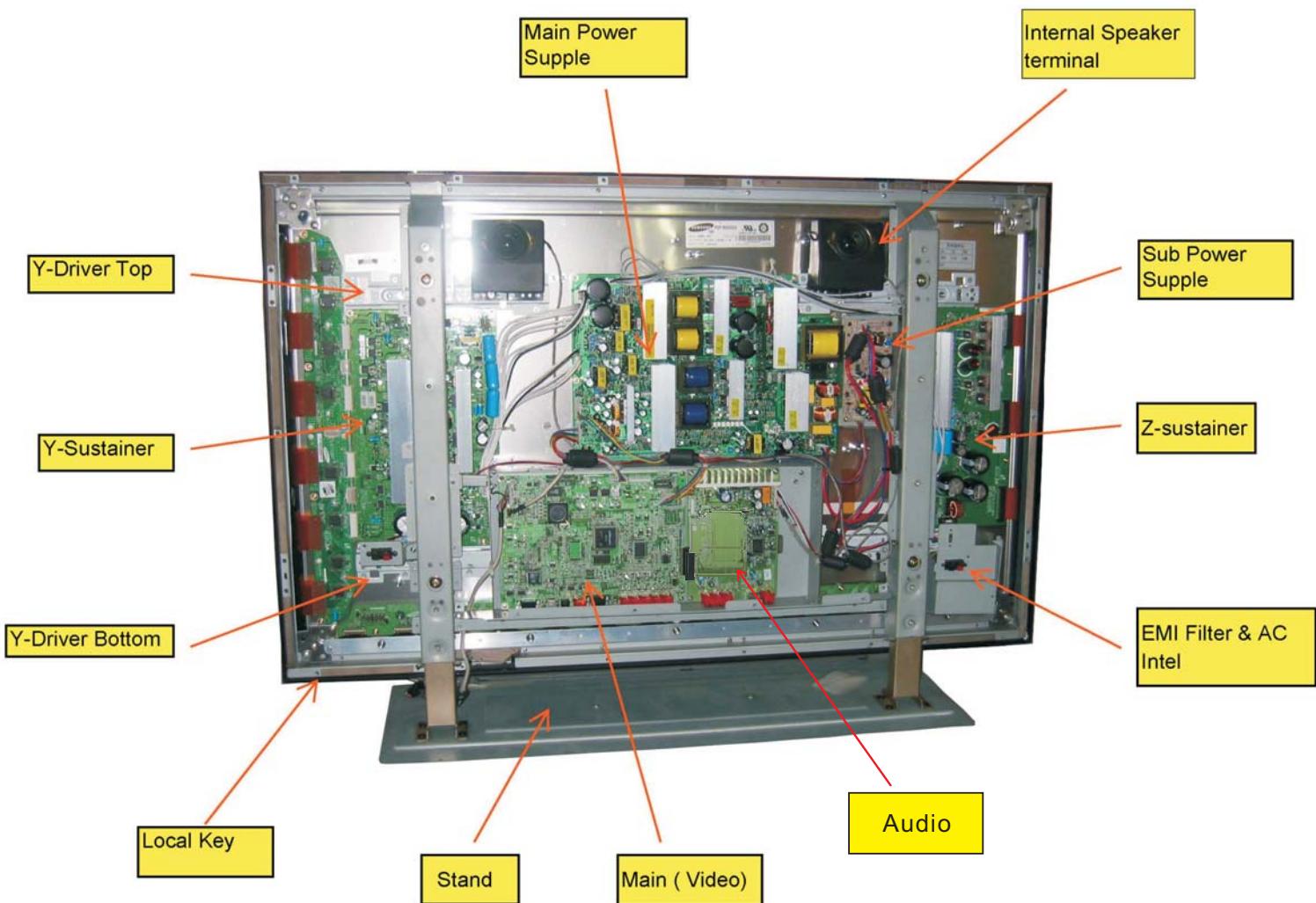
Basic Operations & Circuit Description

MODULE

There are 1 pc. panel and 12 pc.s PCB including 2 pc.s Y/Z Sustainer board, 2 pc.s Y Drive board, 6 pc.s X Extension boards, 1 pc. Control (Signal Input) and 1 pc. Power board in the Module.

SET

There are 6 pc.s PCBs including 1 pc. AUX. PSU Board, 1 pc. Keypad board, 1 pc. Remote Control Receiver board, 1 pc. L/R Speakers and 1 pc. Main (Video) board in the SET.



PCB function

1. Power:
 - (1). Input voltage: AC 100V~120V, 45Hz~60Hz.
Input range: AC 90V(Min)~265V(Max) auto regulation.
 - (2). To provide power for PCBs.
2. Main (Video InterFace) board: To converter TV signals, S signals, AV signals, Y Pb/Cb Pr/Cr signals, DVI signals and D-SUB signals to digital ones and to transmit to Control board.
3. Control board: Dealing with the digital signal for output to panel.
4. Y-Sustainer / Z-Sustainer board:
 - (1). Receiving the signals from Control and high voltage supply.
 - (2). Output scanning waveform for Module.
5. Y-Drive board: Receive signal from Y sustainer, output horizontal scanning waveform to the panel.
6. X extension board (6pcs): Output addressing signals.
7. Tuner/Audio Board: Process and Amplifying the audio signal to speakers and convert TV RF signal to video/audio signal and send to Main board.

PCB failure analysis

1. CONTROL : a. Abnormal noise on screen. b. No picture.
2. MAIN (video) : a. Lacking color, Bad color scale.
b. No voice.
c. No picture but with signals output, OSD and back light.
d. Abnormal noise on screen.
3. POWER : No picture, no power output.
4. Z - Sustainer : a. No picture.
b. Color not enough.
c. Flash on screen.
5. Y - Sustainer : Darker picture with signals.
6. X - Extension : Abormal vertical noise on screen.
7. Audio Board or AUX PSU: a. No voice. (Make sure Mute/OFF) .
b. Noise.

Basic operation of Plasma Display

- 1. After turning on power switch, power board sends 5Vst-by Volt to Micro Processor**
- 2. The micro Processor memorize the last state of Power, When the last state of power is on or receive power on signal from local Key or Remote control, Micro Processor will send on control signal to power. Then Power sends (5Vsc, 9Vsc, 24V and RLYON, Vs ON) to PCBs working. This time VIF will send signals to display Image, OSD on the panel and start to search available signal sources. If the audio signals input, them will be amplified by Audio AMP and transmitted to Speakers.**
- 3. If some abnormal signals are detected (for example: over volts, over current, over temperature and under volts), the system will be shut down by Power off.**

Main IC Specifications

- PW181 Image Processor, Scaler
- PW1231 Digital Video Signal Processor
- VPC 323XD Comb-filter Video Processor
- Z86229 NTSC Line 21 CCD decorder
- MSP34x0G Multistandard Sound Processor
- AD9880 Analog/HDMI Dual Display Interface
- PI5V330 Wideband/Video Quad 2-Channel MUX/DEMUX
- SM5304AV Video Buffer with Built-in Analog LPF
- TDA2616 2 X 12 W hi-fi audio power amplifier with mute
- SAA5360 Multi page intelligent teletext decoder
- AT24C32 Z-Wire Serial EEPROM
- HT48R06A-1 8-Bit Cost-Effective I/O Type MCU

PW181

Product Specification



General Description

The PW181 ImageProcessor is a highly integrated “system-on-a-chip” that interfaces computer graphics and video inputs in virtually any format to a fixed-frequency flat panel display.

Computer and video images from NTSC/PAL to WUXGA at virtually any refresh rate can be resized to fit on a fixed-frequency target display device with any resolution up to WUXGA. Video data from 4:3 aspect ratio NTSC or PAL and 16:9 aspect ratio HDTV or SDTV is supported. Multi-region, nonlinear scaling allows these inputs to be resized optimally for the native resolution of the display.

Advanced scaling techniques are supported, such as format conversion using multiple programmable regions. Three independent image scalers coupled with frame locking circuitry and dual programmable color lookup tables create sharp images in multiple windows, without user intervention.

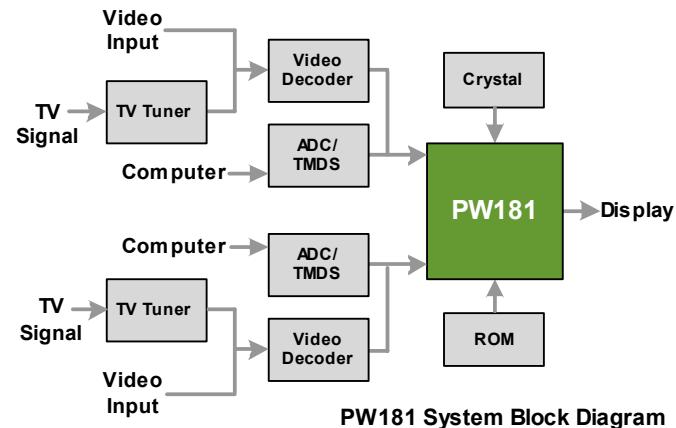
Embedded SDRAM frame buffers and memory controllers perform frame rate conversion and enhanced video processing completely on-chip. A separate memory is dedicated to storage of on-screen display images and CPU general purpose use.

Advanced video processing techniques are supported using the internal frame buffer, including motion adaptive, temporal deinterlacing with film mode detection. When used in combination with the new third-generation scaler, this advanced video processing technology delivers the highest quality video for advanced displays.

Both input ports support integrated DVI 1.0 content protection using standard DVI receivers.

A new advanced OSD Generator with more colors and larger sizes supports more demanding OSD applications, such as on-screen programming guides. When coupled with the new, faster, integrated microprocessor, this OSD Generator supports advanced OSD animation techniques.

Programmable features include the user interface, custom start-up screen, all automatic imaging features, and special screen effects.



Features

- Third-generation, two-dimensional filtering techniques
- Third-generation, advanced scaling techniques
- Second-generation Automatic Image Optimization
- Frame rate conversion
- Video processing
- On-Screen Display (OSD)
- On-chip microprocessor
- JTAG debugger and boundary scan
- Picture-in-picture (PIP)
- Multi-region, non-linear scaling
- Hardware 2-wire serial bus support

Applications

- Multimedia Displays
- Plasma Displays
- Digital Television

Device	Application	Package
PW181-10V	Up to XGA Displays	352 PBGA
PW181-20V	Up to UXGA Displays	



8100 SW Nyberg Road
Tualatin, OR 97062 USA
Telephone: 503.454.1750
FAX: 503.612.0848
www.pixelworks.com

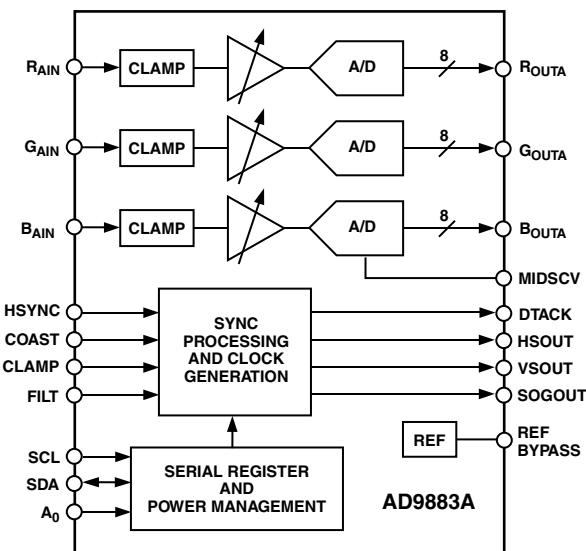
FEATURES

- 140 MSPS Maximum Conversion Rate
- 300 MHz Analog Bandwidth
- 0.5 V to 1.0 V Analog Input Range
- 500 ps p-p PLL Clock Jitter at 110 MSPS
- 3.3 V Power Supply
- Full Sync Processing
- Sync Detect for “Hot Plugging”
- Midscale Clamping
- Power-Down Mode
- Low Power: 500 mW Typical
- 4:2:2 Output Format Mode

APPLICATIONS

- RGB Graphics Processing
- LCD Monitors and Projectors
- Plasma Display Panels
- Scan Converters
- Microdisplays
- Digital TV

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9883A is a complete 8-bit, 140 MSPS monolithic analog interface optimized for capturing RGB graphics signals from personal computers and workstations. Its 140 MSPS encode rate capability and full power analog bandwidth of 300 MHz supports resolutions up to SXGA (1280 × 1024 at 75 Hz).

The AD9883A includes a 140 MHz triple ADC with internal 1.25 V reference, a PLL, and programmable gain, offset, and clamp control. The user provides only a 3.3 V power supply, analog input, and Hsync and COAST signals. Three-state CMOS outputs may be powered from 2.5 V to 3.3 V.

The AD9883A's on-chip PLL generates a pixel clock from the Hsync input. Pixel clock output frequencies range from 12 MHz to

140 MHz. PLL clock jitter is 500 ps p-p typical at 140 MSPS. When the COAST signal is presented, the PLL maintains its output frequency in the absence of Hsync. A sampling phase adjustment is provided. Data, Hsync, and clock output phase relationships are maintained. The AD9883A also offers full sync processing for composite sync and sync-on-green applications.

A clamp signal is generated internally or may be provided by the user through the CLAMP input pin. This interface is fully programmable via a 2-wire serial interface.

Fabricated in an advanced CMOS process, the AD9883A is provided in a space-saving 80-lead LQFP surface-mount plastic package and is specified over the 0°C to 70°C temperature range.

REV. A

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Tel:
Fax:

PW1231A

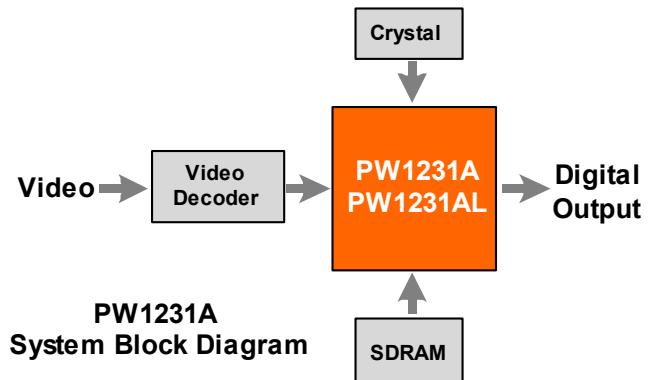
Product Specification



General

The PW1231A is a high-quality, digital video signal processor that incorporates Pixelworks' patented deinterlacing, scaling, and video enhancement algorithms. The PW1231A accepts industry-standard video formats and resolutions, and converts the input into many desired output formats. The highly efficient video algorithms result in excellent quality video.

The PW1231A combines many functions into a single device, including a memory controller, auto-configuration, and others. This high level of integration enables simple, flexible, cost-effective solutions that require fewer components.



Features

- Built-In Memory Controller
- Motion-Adaptive Deinterlace Processor
- Intelligent Edge Deinterlacing
- Digital Color/Luminance Transient Improvement (DCTI/DLTI)
- Interlaced Video Input Options, including NTSC and PAL
- Independent horizontal and vertical scaling
- Copy Protection
- Two-Wire Serial Interface

Applications: For use with Digital Displays

- Flat-Panel (LCD, DLP) TVs
- Rear Projection TVs
- Plasma Displays
- LCD Multimedia Monitors
- Multimedia Projectors

Device	Application	Package
PW1231A PW1231AL	Up to XGA	160-pin PQF

NOTE: "L" denotes lead (Pb) free

pixelworks™

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P/N 001-0097-00 Rev B
July 2003

PRELIMINARY—CONFIDENTIAL

FEATURES

- Analog/HDMI Dual Interface
- Supports High-Bandwidth Digital Content Protection
- RGB to YCbCr two-way color conversion
- Automated clamping level adjustment
- 1.8/3.3V Power Supply
- 100-pin LQFP Pb-Free Package
- RGB and YCbCr Output Formats
- **Analog Interface**
 - 8-bit Triple Analog to Digital Converters
 - 150 MSPS Maximum Conversion Rate
 - Macrovision Detection
 - 2:1 Input Mux
 - Full Sync Processing
 - Sync Detect for "Hot Plugging"
 - Mid-Scale Clamping
- **Digital Video Interface**
 - HDMI 1.0, DVI 1.0
 - 150 MHz HDMI Receiver
 - Supports High-Bandwidth Digital Content Protection (HDCP 1.1)
- **Digital Audio Interface**
 - HDMI 1.0 compatible audio interface
 - S/PDIF (IEC90658 compatible) digital audio output
 - Multi-channel I₂S audio output (up to 8 channels)

APPLICATIONS

- Advanced TV
- HDTV
- Projectors
- LCD Monitor

GENERAL DESCRIPTION

The AD9880 offers designers the flexibility of an analog interface and High-Definition Multimedia Interface (HDMI) receiver integrated on a single chip. Also included is support for High bandwidth Digital Content Protection (HDCP).

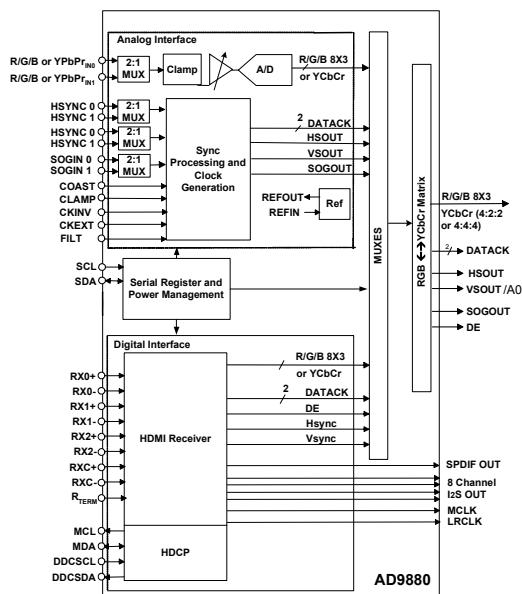
Analog Interface

The AD9880 is a complete 8-bit 150 MSPS monolithic analog interface optimized for capturing Component Video (YPbPr) and RGB graphics signals. Its 150 MSPS encode rate capability and full power analog bandwidth of 300 MHz supports all HDTV formats (up to 1080p) and FPD resolutions up to SXGA (1280 x 1024 at 75 Hz).

The analog interface includes a 150 MHz triple ADC with internal 1.25V reference, a Phase Locked Loop (PLL), and programmable gain, offset, and clamp control. The user provides only 1.8V and 3.3V power supply, analog input, and Hsync. Three-state CMOS outputs may be powered from 1.8V to 3.3V. The AD9880's on-chip PLL generates a pixel clock from Hsync. Pixel clock output frequencies range from 12 MHz to 150 MHz.

AD9880 Preliminary Technical Information

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FUNCTIONAL BLOCK DIAGRAM


PLL clock jitter is typically less than 500 ps p-p at 150 MHz. The AD9880 also offers full sync processing for composite sync and Sync-on-Green (SOG) applications.

Digital Interface

The AD9880 contains a HDMI 1.0 compatible receiver and supports all HDTV formats (up to 1080p) and display resolutions up to SXGA (1280 x 1024 at 75 Hz). The receiver features an intra-pair skew tolerance of up to one full clock cycle. With the inclusion of HDCP, displays may now receive encrypted video content. The AD9880 allows for authentication of a video receiver, decryption of encoded data at the receiver, and renewability of that authentication during transmission as specified by the HDCP 1.1 protocol.

Fabricated in an advanced CMOS process, the AD9880 is provided in a space-saving 100-lead LQFP surface-mount plastic package and is specified over the 0 °C to 70 °C temperature range.

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Comb Filter Video Processor

1. Introduction

The VPC 323xD is a high-quality, single-chip video front-end, which is targeted for 4:3 and 16:9, 50/60-Hz and 100/120 Hz TV sets. It can be combined with other members of the DIGIT3000 IC family (such as DDP 331x) and/or it can be used with 3rd-party products.

The main features of the VPC 323xD are

- high-performance adaptive 4H comb filter Y/C separator with adjustable vertical peaking
- multi-standard color decoder PAL/NTSC/SECAM including all substandards
- four CVBS, one S-VHS input, one CVBS output
- two RGB/YCrCb component inputs, one Fast Blank (FB) input
- integrated high-quality A/D converters and associated clamp and AGC circuits
- multi-standard sync processing
- linear horizontal scaling (0.25 ... 4), as well as non-linear horizontal scaling 'Panoramavision'
- PAL+ preprocessing
- line-locked clock, data and sync, or 656-output interface

- peaking, contrast, brightness, color saturation and tint for RGB/YCrCb and CVBS/S-VHS
- high-quality soft mixer controlled by Fast Blank
- PIP processing for four picture sizes ($\frac{1}{4}$, $\frac{1}{9}$, $\frac{1}{16}$, or $\frac{1}{36}$ of normal size) with 8-bit resolution
- 15 predefined PIP display configurations and expert mode (fully programmable)
- control interface for external field memory
- I²C-bus interface
- one 20.25-MHz crystal, few external components
- 80-pin PQFP package

1.1. System Architecture

Fig.1-1 shows the block diagram of the video processor

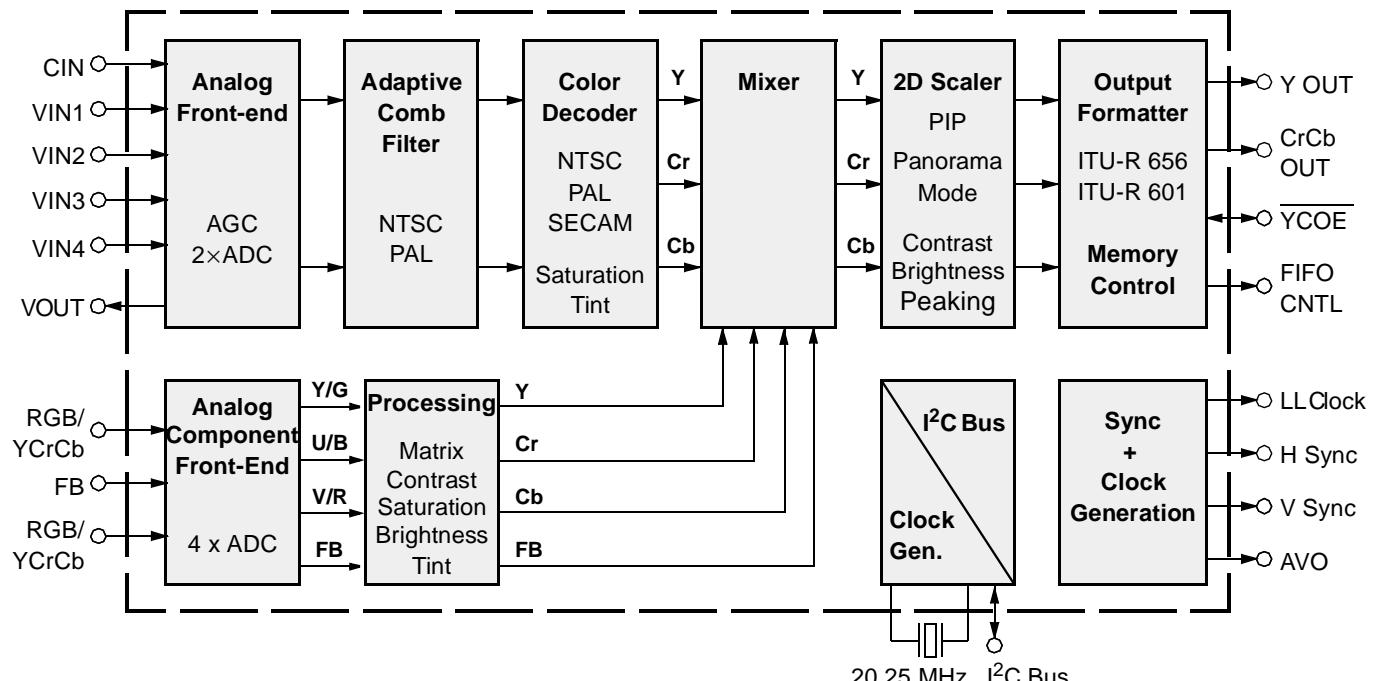


Fig. 1-1: Block diagram of the VPC 323xD



Totally Logical

Z86229

NTSC LINE 21 CCD DECODER

FEATURES

Devices	Speed (MHz)	Pin Count/ Package Types	Standard Temp. Range	Automatic Data Extraction		
				On-Screen Display & Closed Captioning	Program Rating	Time of Day
Z86229	12	18-Pin DIP, SOIC	0°C to + 70°C	Yes	Yes	Yes

- Complete Stand-Alone Line 21 Decoder for Closed-Captioned and Extended Data Services (XDS)
- Preprogrammed to Provide Full Compliance with EIA-608 Specifications for Extended Data Services
- Automatic Extraction and Serial Output of Special XDS Packets (Time of Day, Local Time Zone, and Program Blocking)
- Programmable XDS Filter for a Specific XDS Packet
- Cost-Effective Solution for NTSC Violence Blocking inside Picture-in-Picture (PiP) Windows

- Minimal Communications and Control Overhead Provide Simple Implementation of Violence Blocking, Closed Captioning, and Auto Clock Set Features
- Programmable, On-Screen Display (OSD) for Creating Full Screen OSD or Captions inside a Picture-in-Picture (PiP) Window
- User-Programmable Horizontal Display Position for easy OSD Centering and Adjustment
- I²C Serial Data and Control Communication
- Supports 2 Selectable I²C Addresses

GENERAL DESCRIPTION

Capable of processing Vertical Blanking Interval (VBI) data from both fields of the video frame in data, the Z86229 Line 21 Decoder offers a feature-rich solution for any television or set-top application. The robust nature of the Z86229 helps the device conform to the transmission format defined in the Television Decoder Circuits Act of 1990, and in accordance with the Electronics Industry Association specification 608 (EIA-608).

The Line 21 data stream can consist of data from several data channels multiplexed together. Field 1 consists of four data channels: two Captions and two Texts. Field 2 consists of five additional data channels: two Captions, two Texts, and Extended Data Services (XDS). The XDS data structure is

defined in EIA-608. The Z86229 can recover and display data transmitted on any of these nine data channels.

The Z86229 can recover and output to a host processor via the I²C serial bus. The recovered XDS data packet is further defined in the EIA-608 specification. The on-chip XDS filters in the Z86229 are fully programmable, enabling recovery of only those XDS data packets selected by the user. This functionality allows the device to extract the required XDS information with proper XDS filter setup for compatibility in a variety of TVs, VCRs, and Set-Top boxes.

In addition, the Z86229 is ideally suited to monitor Line 21 video displayed in a PiP window for violence blocking, CCD, and other XDS data services. A block diagram of the Z86229 is illustrated in Figure 1.

Multistandard Sound Processor Family

Release Note: Revision bars indicate significant changes to the previous edition. The hardware and software description in this document is valid for the MSP 34x0G version B8 and following versions.

1. Introduction

The MSP 34x0G family of single-chip Multistandard Sound Processors covers the sound processing of all analog TV-Standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed on a single chip. Figure 1-1 shows a simplified functional block diagram of the MSP 34x0G.

This new generation of TV sound processing ICs now includes versions for processing the multichannel television sound (MTS) signal conforming to the standard recommended by the Broadcast Television Systems Committee (BTSC). The DBX noise reduction, or alternatively, Micronas Noise Reduction (MNR) is performed alignment free.

Other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM Stereo Radio standard.

Current ICs have to perform adjustment procedures in order to achieve good stereo separation for BTSC and EIA-J. The MSP 34x0G has optimum stereo performance without any adjustments.

All MSP 34xxG versions are pin compatible to the MSP 34xxD. Only minor modifications are necessary to adapt a MSP 34xxD controlling software to the MSP 34xxG. The MSP 34x0G further simplifies controlling software. Standard selection requires a single I²C transmission only.

The MSP 34x0G has built-in automatic functions: The IC is able to detect the actual sound standard automatically (Automatic Standard Detection). Furthermore, pilot levels and identification signals can be evaluated internally with subsequent switching between mono/stereo/bilingual; no I²C interaction is necessary (Automatic Sound Selection).

The MSP 34x0G can handle very high FM deviations even in conjunction with NICAM processing. This is especially important for the introduction of NICAM in China.

The ICs are produced in submicron CMOS technology. The MSP 34x0G is available in the following packages: PLCC68 (not intended for new design), PSDIP64, PSDIP52, PQFP80, and PLQFP64.

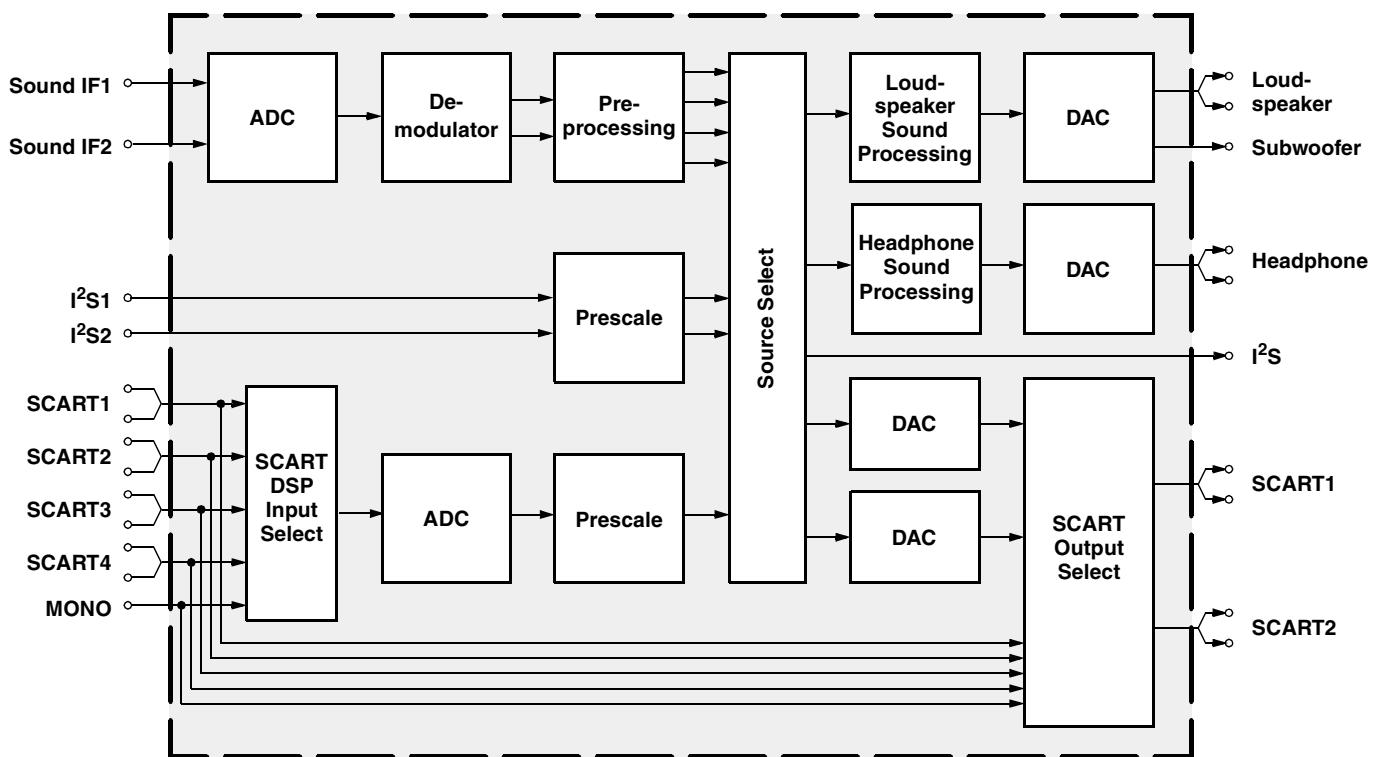


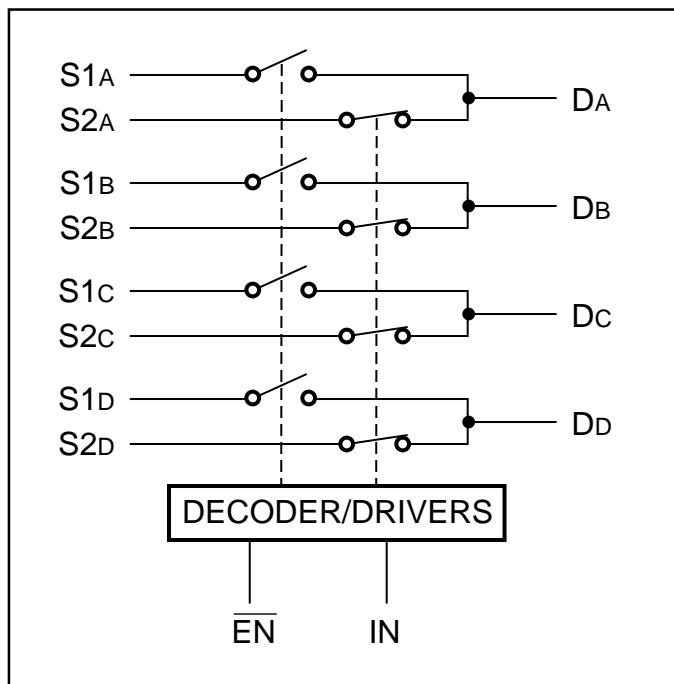
Fig. 1-1: Simplified functional block diagram of the MSP 34x0G

Low ON Resistance Wideband/Video Quad 2-Channel MUX/DEMUX

Product Features:

- High-performance, low-cost solution to switch between video sources
- Wide bandwidth: 200 MHz
- Low ON-resistance: 3Ω
- Low crosstalk at 10 MHz: -58 dB
- Ultra-low quiescent power (0.1 μ A typical)
- Single supply operation: +5.0V
- Fast switching: 10 ns
- High-current output: 100 mA
- Packages available:
 - 16-pin 300-mil wide plastic SOIC (S)
 - 16-pin 150-mil wide plastic SOIC (W)
 - 16-pin 150-mil wide plastic QSOP (Q)

Functional Block Diagram



Truth Table

\overline{EN}	IN	ON Switch
0	0	S1A, S1B, S1C, S1D
0	1	S2A, S2B, S2C, S2D
1	X	Disabled

Product Description:

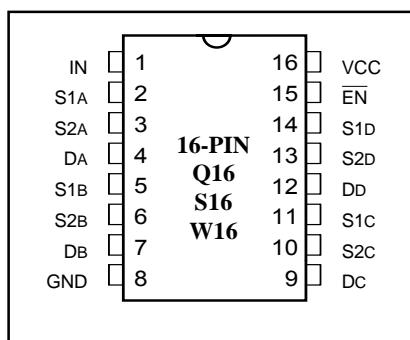
Pericom Semiconductor's PI5V series of mixed signal video circuits are produced in the Company's advanced CMOS low-power technology, achieving industry leading performance.

The PI5V330 is a true bidirectional Quad 2-channel multiplexer/demultiplexer that is recommended for both RGB and composite video switching applications. The VideoSwitch™ can be driven from a current output RAMDAC or voltage output composite video source.

Low ON-resistance and wide bandwidth make it ideal for video and other applications. Also this device has exceptionally high current capability which is far greater than most analog switches offered today. A single 5V supply is all that is required for operation.

The PI5V330 offers a high-performance, low-cost solution to switch between video sources. The application section describes the PI5V330 replacing the HC4053 multiplier and buffer/amplifier.

16-Pin Product Configuration



Product Pin Description

Pin Name	Description
S1A, S2A S1B, S2B S1C, S2C S1D, S2D	Analog Video I/O
IN	Select Input
\overline{EN}	Enable
DA, DB, DC, DD	Analog Video I/O
GND	Ground
VCC	Power

OVERVIEW

The SM5304AV is a 75Ω terminating resistance drive video buffer with built-in analog filter. The filter cutoff frequency, controlled by the resistance connected to RFC pin, can be set to match any system resolution. The output buffer can be selected 0dB, 6dB, and 12dB. The feedback point occurs after the external coupling capacitors, and the coupling capacitances can be reduced.

FEATURES

- 5V \pm 10% supply voltage
- Adjustable cutoff frequency using external resistor
- 0dB, 6dB, 12dB selectable gain using logic signal
- ± 0.5 dB output gain error
- Two systems (two load resistances) can be driven
- 0.7% output signal harmonic distortion
- Sag compensation circuit built-in
- Package: 8-pin VSOP (Pb free)

APPLICATIONS

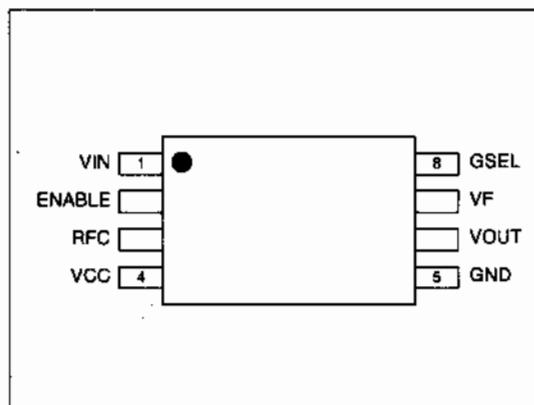
- DVD
- Digital still camera
- Digital VHS

ORDERING INFORMATION

Device	Package
SM5304AV	8-pin VSOP

PINOUT

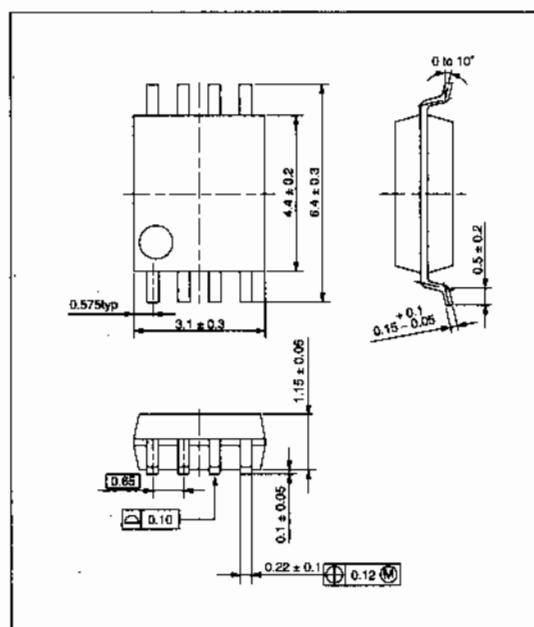
(Top view)



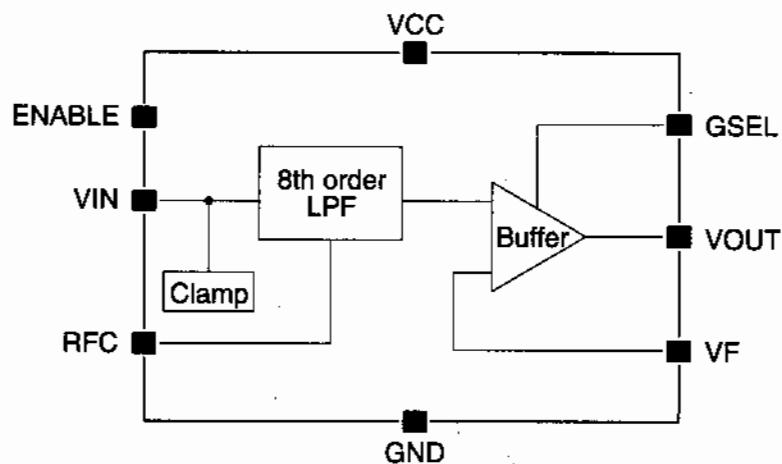
PACKAGE DIMENSIONS

(Unit: mm)

Weight: 0.04g



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	IO ¹	A/D ²	Description
1	VIN	I	A	Input signal pin
2	ENABLE	I	D	Enable signal input pin (with pull-down resistor)
3	RFC	O	A	LPF cutoff frequency set pin
4	VCC	-	-	5V supply pin
5	GND	-	-	Ground pin
6	VOUT	O	A	Output signal pin
7	VF	I	A	Output signal feedback pin for sag compensation circuit
8	GSEL	I	D	Gain set signal input pin

1. I: input, O: output

2. A: analog, D: digital

2 x 12 W hi-fi audio power amplifiers with mute

TDA2616/TDA2616Q

FEATURES

- Requires very few external components
- No switch-on/switch-off clicks
- Input mute during switch-on and switch-off
- Low offset voltage between output and ground
- Excellent gain balance of both amplifiers
- Hi-fi in accordance with IEC 268 and DIN 45500
- Short-circuit proof and thermal protected
- Mute possibility.

GENERAL DESCRIPTION

The TDA2616 and TDA2616Q are dual power amplifiers. The TDA2616 is supplied in a 9-lead single-in-line (SIL9) plastic power package (SOT131), while the TDA2616Q is supplied in a 9-lead SIL-bent-to-DIL plastic power package (SOT157). They have been especially designed for mains fed applications, such as stereo radio and stereo TV.

QUICK REFERENCE DATA

Stereo application

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\pm V_p$	supply voltage range		7.5	—	21	V
P_o	output power	$V_p = \pm 16$ V; THD = 0.5%	—	12	—	W
G_v	internal voltage gain		—	30	—	dB
$ G_v $	channel unbalance		—	0.2	—	dB
α	channel separation		—	70	—	dB
SVRR	supply voltage ripple rejection		—	60	—	dB
V_{no}	noise output voltage		—	70	—	μ V

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA2616	9	SIL	plastic	SOT131 ⁽¹⁾
TDA2616Q	9	SIL-bent-to-DIL	plastic	SOT157 ⁽²⁾

Notes

1. SOT131-2; 1996 August 27.
2. SOT157-2; 1996 August 27.

2 x 12 W hi-fi audio power amplifiers with mute

TDA2616/TDA2616Q

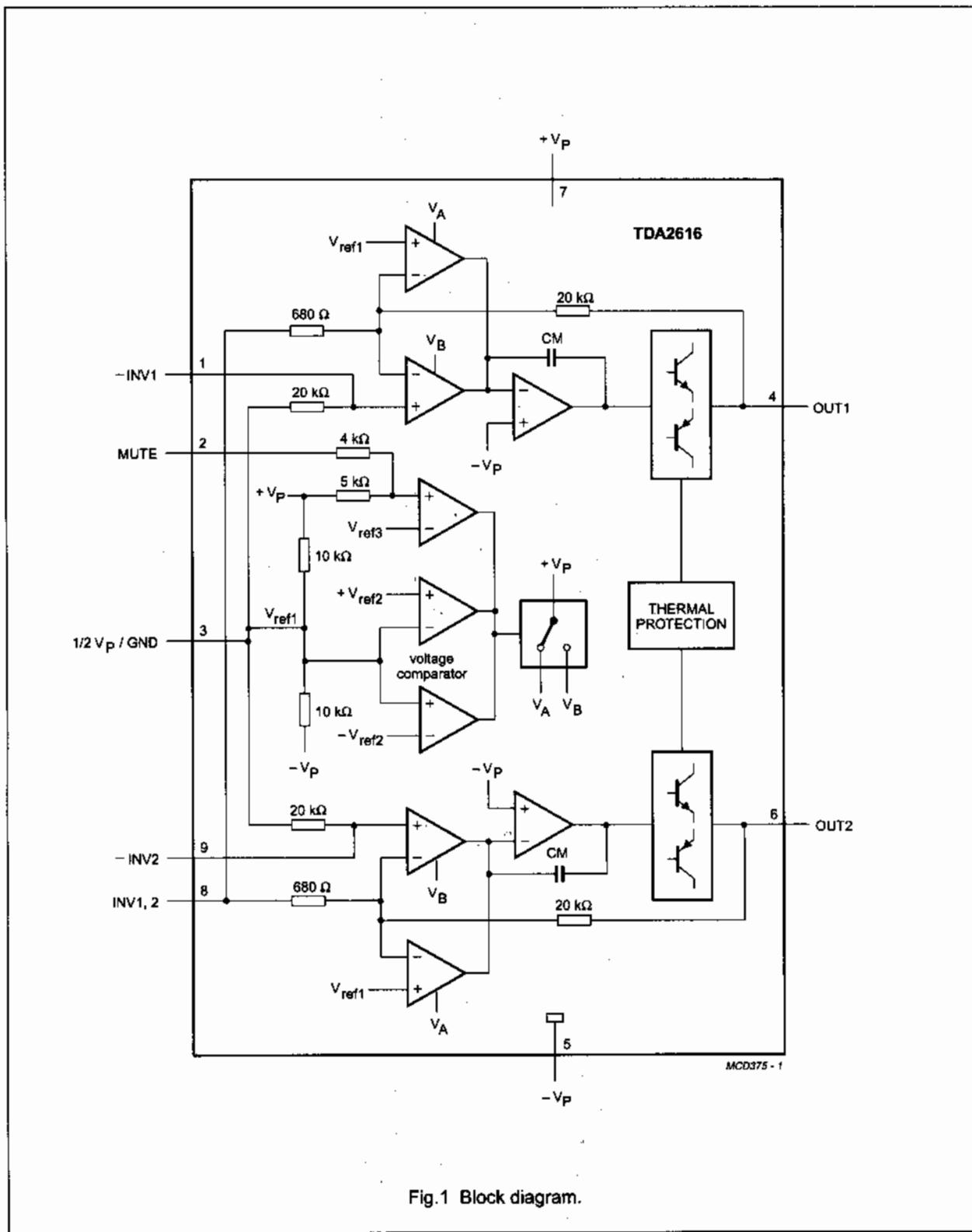


Fig.1 Block diagram.

Multi page intelligent teletext decoder

SAA5360; SAA5361

1 FEATURES

- Support for 50 or 60 and 100 or 120 Hz and progressive scan display modes
- Complete 625 line teletext decoder in one chip reduces printed-circuit board area and cost
- Automatic detection of transmitted fastext links or service information (packet 8/30)
- On-Screen Display (OSD) for user interface menus using teletext and dedicated menu icons
- Video Programming System (VPS) decoding
- Wide Screen Signalling (WSS) decoding
- Pan-European, Cyrillic, Greek, Turkish, Arabic and Iranian character sets in each chip
- High-level command interface via I²C-bus gives easy control with a low software overhead
- High-level command interface is backward compatible to Stand-Alone Fastext And Remote Interface (SAFARI)
- 625 and 525 line display
- RGB interface to standard colour decoder ICs; current source
- Versatile 8-bit open-drain Input/Output (I/O) expander; 5 V tolerant
- Single 12 MHz crystal oscillator
- Single power supply: from 3.0 V to 3.6 V
- Operating temperature: -20 to +70 °C
- Automatic detection of transmitted pages to be selected by page up and page down



- 8 page fastext decoder
- Table Of Pages (TOP) decoder with Basic Top Table (BTT) and Additional Information Tables (AITs)
- 4 page user-defined list mode.

2 GENERAL DESCRIPTION

The SAA5360; SAA5361 is a single-chip multi page 625 line world system teletext decoder with a high-level command interface, and is SAFARI compatible.

The device is designed to minimize the overall system cost, due to the high-level command interface offering the benefit of a low software overhead in the TV microcontroller.

The SAA5360 incorporates the following functions:

- 10 page teletext decoder with OSD, fastext, TOP, default and list acquisition modes
- Automatic channel installation support.

The functionality of the SAA5361 is similar to the SAA5360, but offers the capability to store up to 250 additional pages of teletext in an external SRAM.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{DD}	all supply voltages	referenced to V _{SS}	3.0	3.3	3.6	V
I _{DDP}	periphery supply current	note 1	1	—	—	mA
I _{DCC}	core supply current	normal mode	—	15	18	mA
		idle mode	—	4.6	6	mA
I _{DCA}	analog supply current	normal mode	—	45	48	mA
		idle mode	—	0.87	1	mA
f _{xtal(nom)}	nominal crystal frequency	fundamental mode	—	12	—	MHz
T _{amb}	ambient temperature		-20	—	+70	°C
T _{stg}	storage temperature		-55	—	+125	°C

Note

1. Periphery supply current is dependent on external components and I/O voltage levels.

Multi page intelligent teletext decoder

SAA5360; SAA5361

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA5360HL	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
SAA5361HL	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

5 BLOCK DIAGRAM

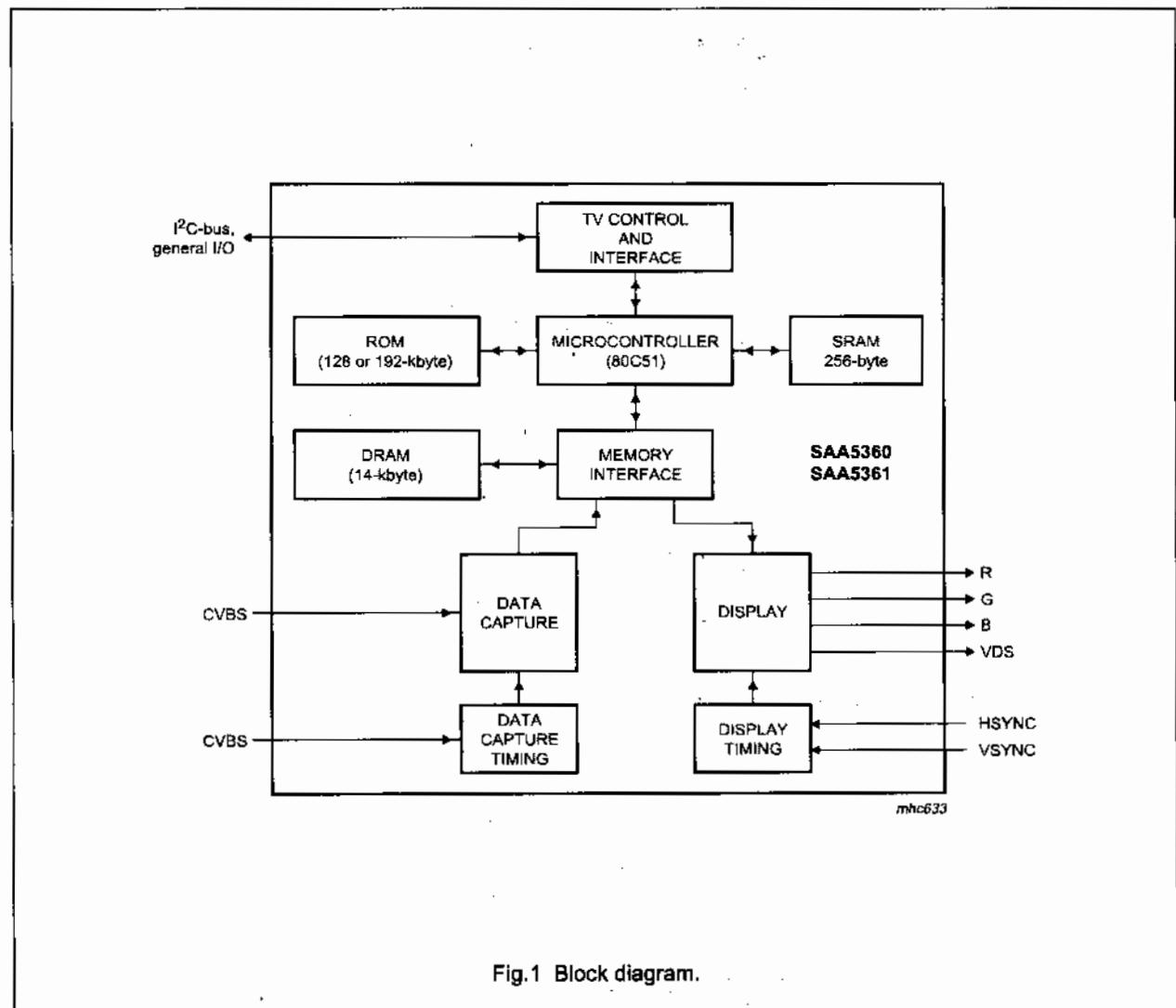


Fig.1 Block diagram.

Features

- **Low-Voltage and Standard-Voltage Operation**
 - 5.0 ($V_{CC} = 4.5V$ to 5.5V)
 - 2.7 ($V_{CC} = 2.7V$ to 5.5V)
 - 2.5 ($V_{CC} = 2.5V$ to 5.5V)
 - 1.8 ($V_{CC} = 1.8V$ to 5.5V)
- **Low-Power Devices ($I_{SB} = 2 \mu A$ @ 5.5V) Available**
- **Internally Organized 4096 x 8, 8192 x 8**
- **2-Wire Serial Interface**
- **Schmitt Trigger, Filtered Inputs for Noise Suppression**
- **Bidirectional Data Transfer Protocol**
- **100 kHz (1.8V, 2.5V, 2.7V) and 400 kHz (5V) Clock Rate**
- **Write Protect Pin for Hardware Data Protection**
- **32-Byte Page Write Mode (Partial Page Writes Allowed)**
- **Self-Timed Write Cycle (10 ms max)**
- **High Reliability**
 - Endurance: 1 Million Write Cycles
 - Data Retention: 100 Years
 - ESD Protection: >3,000V
- **Automotive Grade and Extended Temperature Devices Available**
- **8-Pin JEDEC PDIP, 8-Pin JEDEC SOIC, 8-Pin EIAJ SOIC, and 8-pin TSSOP Packages**

Description

The AT24C32/64 provides 32,768/65,536 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 4096/8192 words of 8 bits each. The device's cascadable feature allows up to 8 devices to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C32/64 is available in space saving 8-pin JEDEC PDIP, 8-pin JEDEC SOIC, 8-pin EIAJ SOIC, and 8-pin TSSOP (AT24C64) packages and is accessed via a 2-wire serial interface. In addition, the entire family is available in 5.0V (4.5V to 5.5V), 2.7V (2.7V to 5.5V), 2.5V (2.5V to 5.5V) and 1.8V (1.8V to 5.5V) versions.

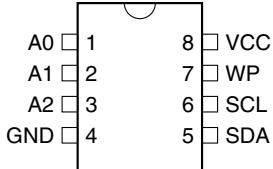
Pin Configurations

Pin Name	Function
A0 - A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect

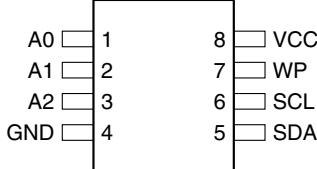
8-Pin TSSOP



8-Pin PDIP



8-Pin SOIC



2-Wire Serial EEPROM

32K (4096 x 8)

64K (8192 x 8)

AT24C32

AT24C64

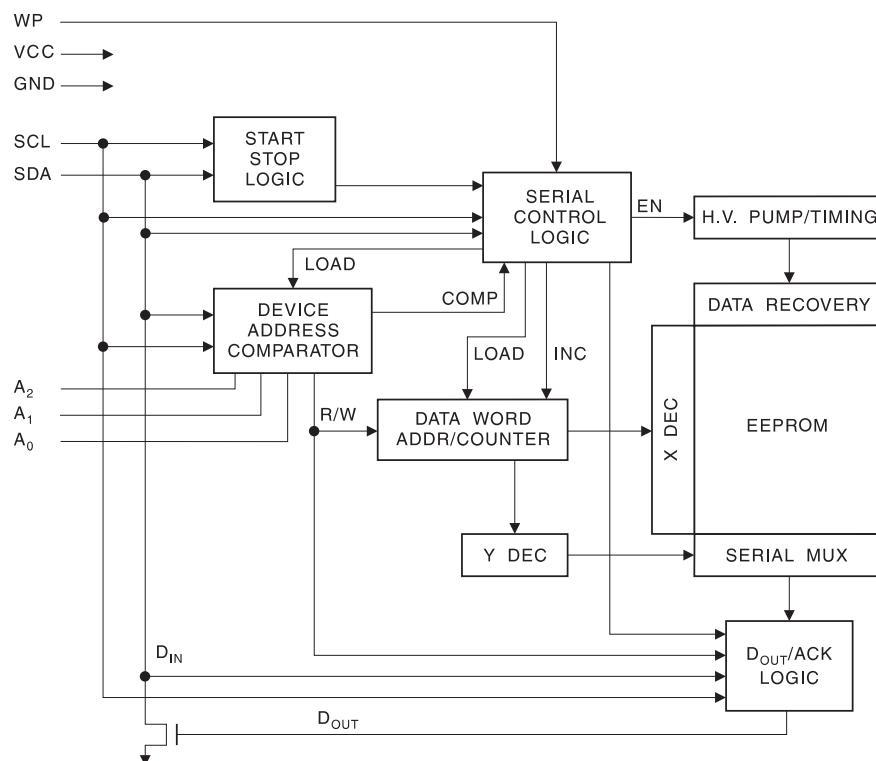


Absolute Maximum Ratings*

Operating Temperature.....	-55°C to +125°C
Storage Temperature.....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current.....	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

DEVICE/PAGE ADDRESSES (A₂, A₁, A₀): The A₂, A₁ and A₀ pins are device address inputs that are hard wired or left not connected for hardware compatibility with AT24C16. When the pins are hardwired, as many as eight 32K/64K devices may be addressed on a single bus system (device addressing is discussed in detail under the

Device Addressing section). When the pins are not hardwired, the default A₂, A₁, and A₀ are zero.

WRITE PROTECT (WP): The write protect input, when tied to GND, allows normal write operations. When WP is tied high to V_{CC}, all write operations to the upper quadrant (8/16K bits) of memory are inhibited. If left unconnected, WP is internally pulled down to GND.

Memory Organization

AT24C32/64, 32K/64K SERIAL EEPROM: The 32K/64K is internally organized as 256 pages of 32 bytes each. Random word addressing requires a 12/13 bit data word address.

Features

- Operating voltage:
 $f_{sys}=4MHz$: 2.2V~5.5V
 $f_{sys}=8MHz$: 3.3V~5.5V
- 13 bidirectional I/O lines
- An interrupt input shared with an I/O line
- 8-bit programmable timer/event counter with overflow interrupt and 8-stage prescaler
- On-chip crystal and RC oscillator
- Watchdog Timer
- 1024×14 program memory ROM
- 64×8 data memory RAM
- Buzzer driving pair and PFD supported

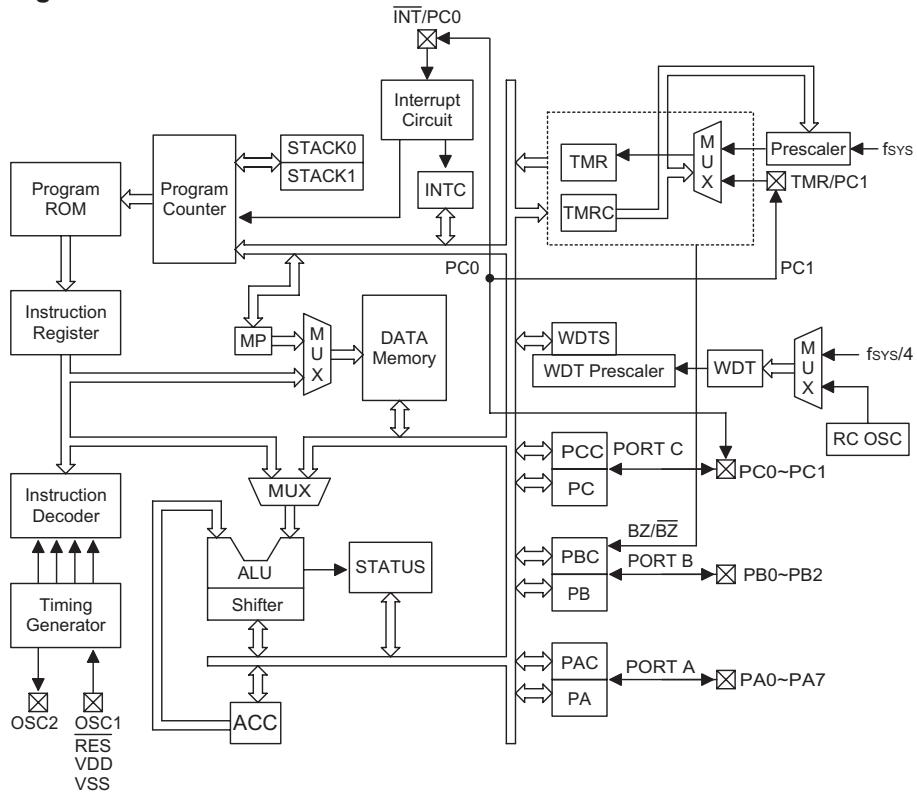
- HALT function and wake-up feature reduce power consumption
- Up to 0.5 μ s instruction cycle with 8MHz system clock at $V_{DD}=5V$
- All instructions in one or two machine cycles
- 14-bit table read instruction
- Two-level subroutine nesting
- Bit manipulation instruction
- 63 powerful instructions
- Low voltage reset function
- 16-pin SSOP package
18-pin DIP/SOP package

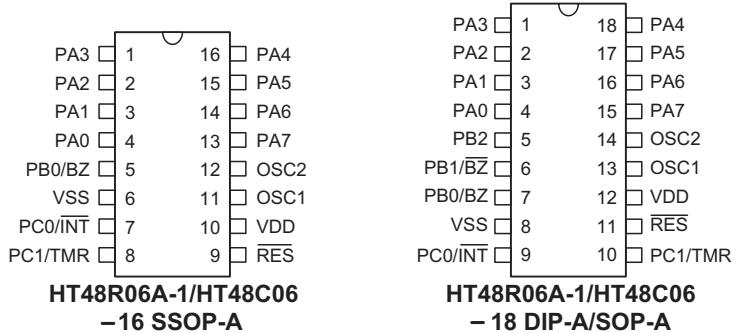
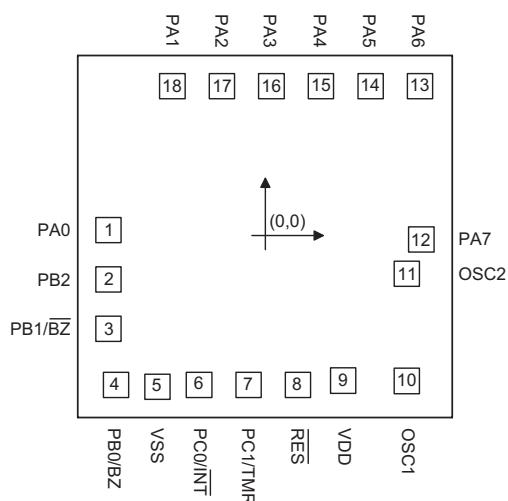
General Description

The HT48R06A-1/HT48C06 are 8-bit high performance, RISC architecture microcontroller devices specifically designed for cost-effective multiple I/O control product applications. The mask version HT48C06 is fully pin and functionally compatible with the OTP version HT48R06A-1 device.

The advantages of low power consumption, I/O flexibility, timer functions, oscillator options, HALT and wake-up functions, watchdog timer, buzzer driver, as well as low cost, enhance the versatility of these devices to suit a wide range of application possibilities such as industrial control, consumer products, subsystem controllers, etc.

Block Diagram



Pin Assignment

Pad Assignment
HT48C06


* The IC substrate should be connected to VSS in the PCB layout artwork.

Pad Description

Pad Name	I/O	Options	Description
PA0~PA7	I/O	Pull-high* Wake-up	Bidirectional 8-bit input/output port. Each bit can be configured as wake-up input by options. Software instructions determine the CMOS output or Schmitt trigger input with a pull-high resistor (determined by pull-high options).
PB0/ <u>BZ</u> PB1/ <u>BZ</u> PB2	I/O	Pull-high* I/O or BZ/ <u>BZ</u>	Bidirectional 3-bit input/output port. Software instructions determine the CMOS output or Schmitt trigger input with a pull-high resistor (determined by pull-high options). The PB0 and PB1 are pin-shared with the BZ and <u>BZ</u> , respectively. Once the PB0 and PB1 are selected as buzzer driving outputs, the output signals come from an internal PFD generator (shared with a timer/event counter).
VSS	—	—	Negative power supply, ground
PC0/ <u>INT</u> PC1/TMR	I/O	Pull-high*	Bidirectional I/O lines. Software instructions determine the CMOS output or Schmitt trigger input with a pull-high resistor (determined by pull-high options). The external interrupt and timer input are pin-shared with the PC0 and PC1, respectively. The external interrupt input is activated on a high to low transition.
RES	I	—	Schmitt trigger reset input. Active low
VDD	—	—	Positive power supply
OSC1 OSC2	I O	Crystal or RC	OSC1, OSC2 are connected to an RC network or Crystal (determined by options) for the internal system clock. In the case of RC operation, OSC2 is the output terminal for 1/4 system clock.

* All pull-high resistors are controlled by an option bit.

Absolute Maximum Ratings

Supply Voltage	V _{SS} −0.3V to V _{SS} +6.0V	Storage Temperature	−50°C to 125°C
Input Voltage.....	V _{SS} −0.3V to V _{DD} +0.3V	Operating Temperature	−40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V _{DD}	Conditions				
V _{DD}	Operating Voltage	—	f _{SYS} =4MHz	2.2	—	5.5	V
		—	f _{SYS} =8MHz	3.3	—	5.5	V
I _{DD1}	Operating Current (Crystal OSC)	3V	No load, f _{SYS} =4MHz	—	0.6	1.5	mA
		5V		—	2	4	mA
I _{DD2}	Operating Current (RC OSC)	3V	No load, f _{SYS} =4MHz	—	0.8	1.5	mA
		5V		—	2.5	4	mA
I _{DD3}	Operating Current (Crystal OSC)	5V	No load, f _{SYS} =8MHz	—	3	5	mA
I _{STB1}	Standby Current (WDT Enabled)	3V	No load, system HALT	—	—	5	μA
		5V		—	—	10	μA
I _{STB2}	Standby Current (WDT Disabled)	3V	No load, system HALT	—	—	1	μA
		5V		—	—	2	μA
V _{IL1}	Input Low Voltage for I/O Ports, TMR and INT	—	—	0	—	0.3V _{DD}	V
V _{IH1}	Input High Voltage for I/O Ports, TMR and INT	—	—	0.7V _{DD}	—	V _{DD}	V
V _{IL2}	Input Low Voltage (RES)	—	—	0	—	0.4V _{DD}	V
V _{IH2}	Input High Voltage (RES)	—	—	0.9V _{DD}	—	V _{DD}	V
V _{LVR}	Low Voltage Reset	—	LVR enabled	2.7	3.0	3.3	V
I _{OL}	I/O Port Sink Current	3V	V _{OL} =0.1V _{DD}	4	8	—	mA
		5V		10	20	—	mA
I _{OH}	I/O Port Source Current	3V	V _{OH} =0.9V _{DD}	-2	-4	—	mA
		5V		-5	-10	—	mA
R _{PH}	Pull-high Resistance	3V	—	40	60	80	kΩ
		5V	—	10	30	50	kΩ

DATE: Jun 24, 2005

CUSTOMER'S A/S MANUAL

107cm (42 Inch) Wide Plasma Display Module

MODEL : 42 SD V4 PDP

(S42SD-YD07)

Quality Innovation Team

PDP Division, Samsung SDI

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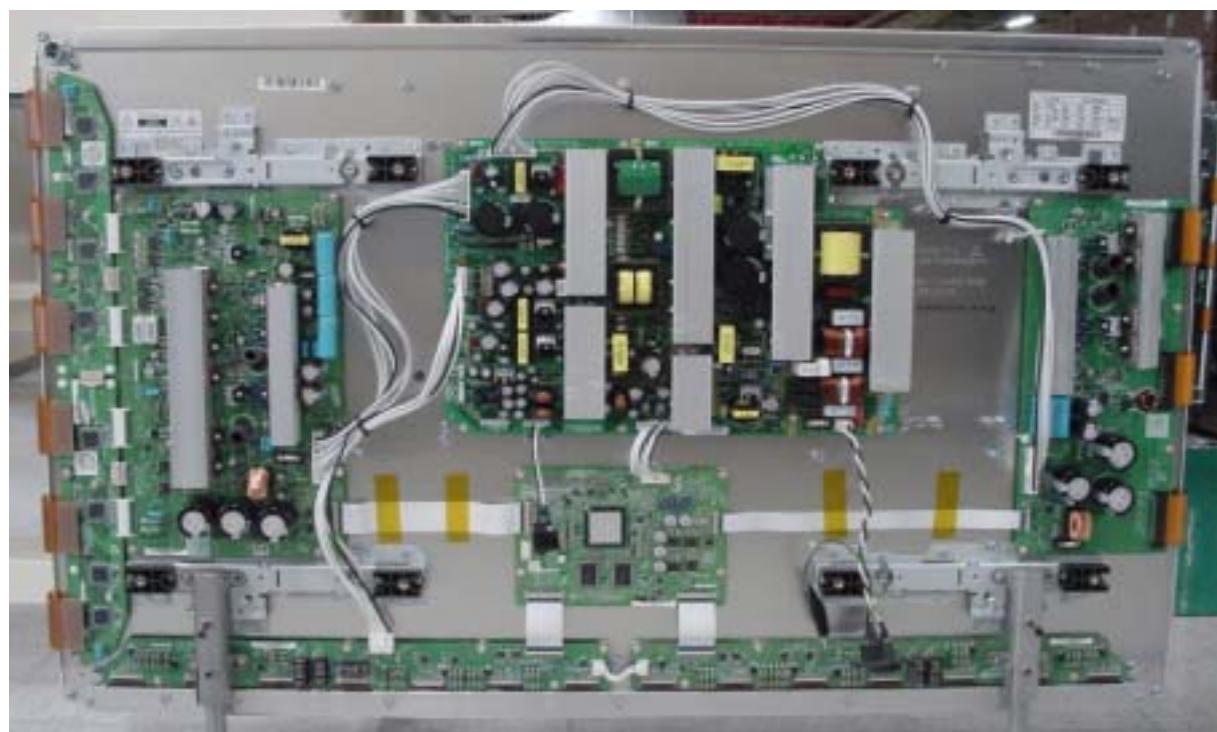
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1. Overview

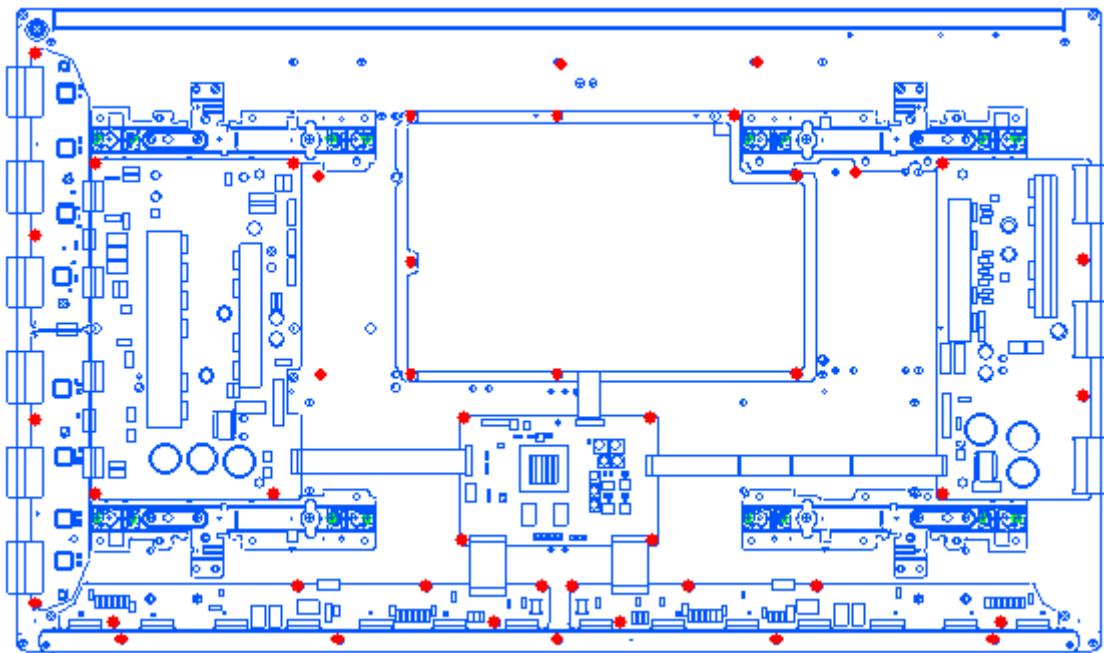
1-1 Model Name of Plasma Display

MODEL : 42 SD V4 PDP (S42SD-YD07)

1-2 External View



【 M3 = X Board + Y Board + Logic Board + SMPS 】

1-3 Points of Screw Mount

Green Dot : SCREW 4X12

Red Dot : SCREW 3X10

1-4 Specifications

No	Item	Specification	
1	Pixel	852 (H) × 480 (V) pixels (1 pixel = 1 R,G,B cells)	
2	Number of Cells	2556 (H) × 480 (V)	
3	Pixel Pitch	1.095 (H) mm × 1.110 (V) mm	
4	Cell Pitch	R	0.365 (H) mm × 1.110 (V) mm
		G	0.365 (H) mm × 1.110 (V) mm
		B	0.365 (H) mm × 1.110 (V) mm
5	Display size	932.940 (H) mm × 532.800(V) mm [36.73 inch × 20.98 inch]	
6	Screen size	Diagonal 42" Color Plasma Display Module	
7	Screen aspect	16 : 9	
8	Display color	16.77 million colors	
9	Viewing angle	Over 160° (Angle with 50% and greater brightness perpendicular to PDP module)	
10	Dimensions	982 (W) × 582 (H) × 54 (D) mm	
11	Weight	Module 1	About 15.4 kg
12	Packing weight	Module 1	233kg ± 5kg (including modules) / 11pcs/BOX
13	Packing size	L 1175 * W 1140 * H 893 (mm) / 11pcs/BOX	
14	Broadcasting reception Vertical frequency and Video/Logic Interface	60Hz/ 50Hz, LVDS	

2. PRECAUTIONS

**** To prevent the risks of unit damage, electrical shock and radiation, take the following safety, service, and ESD precautions.**

2-1 Handling Precautions for Plasma Display

- PDP module use high voltage that is dangerous to human. Before operating PDP, always check the dust to prevent circuit short. Be careful touching the circuit device when power is on.
- PDP module is sensitive to dust and humidity. Therefore, assembling and disassembling must be done in no dust place.
- PDP module has a lot of electric devices. Service engineer must wear equipment(for example , earth ring) to prevent electric shock and working clothes to prevent electrostatic.
- PDP module use a fine pitch connector which is only working by exactly connecting with flat cable. Operator must pay attention to a complete connection when connector is reconnected after repairing.
- The capacitor's remaining voltage in the PDP module's circuit board temporarily remains after power is off. Operator must wait for discharging of remaining voltage during at least 1 minute.

2-2 Safety Precautions for Service (Handling, prevention of a electrical shock, measure against power outage, etc)

(Safety Precautions)

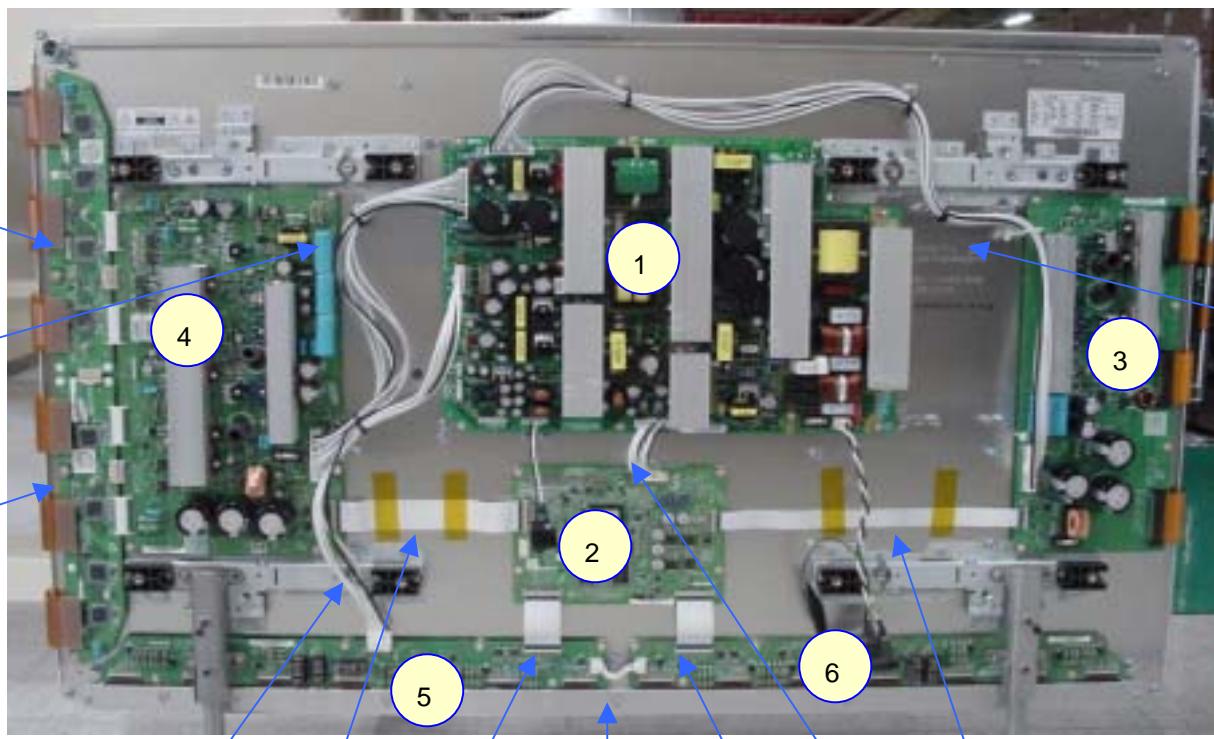
- Before replacing a board, discharge forcibly The remaining electricity from board.
- When connecting FFC and TCPs to the module, recheck that they are perfectly connected.
- To prevent electrical shock, be careful not to touch leads during circuit operations.
- To prevent the Logic circuit from being damaged due to wrong working, do not connect/disconnect signal cables during circuit operations.

- Do thoroughly adjustment of a voltage label and voltage-insulation.
- Before reinstalling the chassis and the chassis assembly, be sure to use all protective stuffs including a nonmetal controlling handle and the covering of partitioning type.
- Caution for design change : Do not install any additional devices to the module, and do not change the electrical circuit design.
- For example: Do not insert a subsidiary audio or video connector. If you insert It, It cause danger on safety. And, If you change the design or insert, Manufactor guarantee will be not effect. .
- If any parts of wire is overheats of damaged, replace it with a new specified one immediately, and identify the cause of the problem and remove the possible dangerous factors.
- Examine carefully the cable status if it is twisted or damaged or displaced. Do not change the space between parts and circuit board. Check the cord of AC power preparing damage.
- Product Safety Mark : Some of electric or implement material have special characteristics invisible that was related on safety. In case of the parts are changed with new one, even though the Voltage and Watt is higher than before, the Safety and Protection function will be lost.
- The AC power always should be turned off, before next repair..
- Check assembly condition of screw, parts and wire arrangement after repairing. Check whether the material around the parts get damaged.

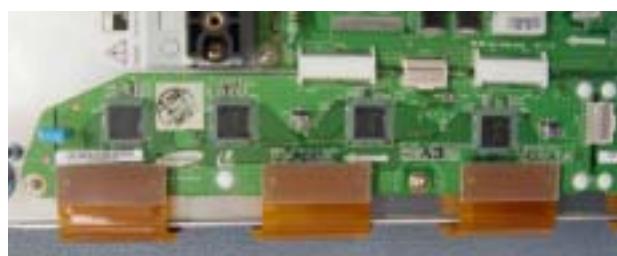
(Precaution when repairing ESD)

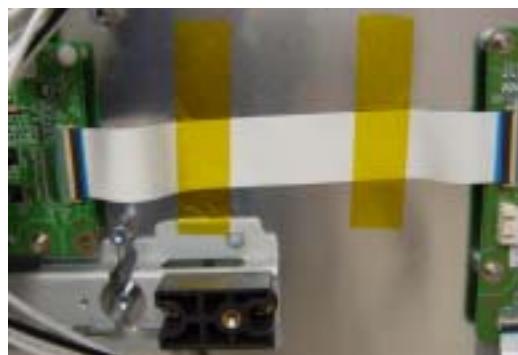
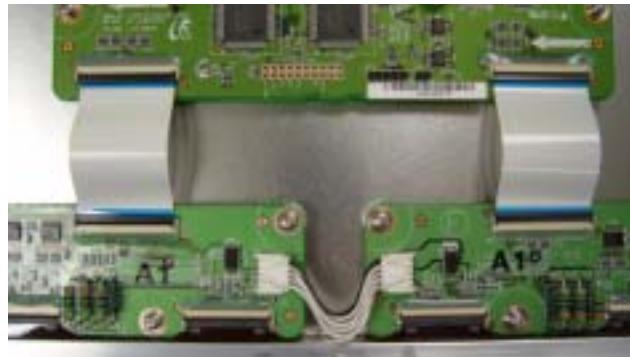
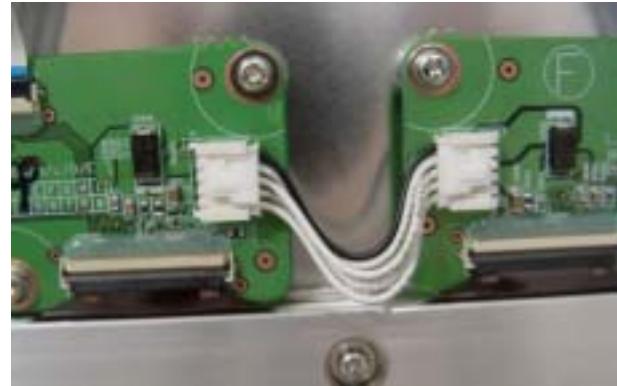
- There is ESD which is easily damaged by electrostatics.(for example Integrated circuit, FET) Electrostatic damage rate of product will be reduced by the following technics electric by ground connection, or must wear the antistatic wrist-belt and ring. (It must be operated after removing dust on it – It comes under precaution of electric shock.)
- Before handling semiconductor parts/assembly, must remove positive

- After removing ESD assembly, put on it with aluminum stuff on the conductive surface to prevent charging.
- Do not use chemical stuff using Freon. It generates positive electric that can damage ESD.
- Must use a soldering device for ground-tip when soldering or de-soldering ESD.
- Must use anti-static solder removal device. Most removal device do not have antistatic which can charge a enough positive electric enough damaging ESD.
- Before removeing the protective material from the lead of a new ESD, bring the protective material into contact with the chassis or assembly that the ESD is to be installed on.
- When handing an unpacked ESD for replacement, do not move around too much. Moving (legs on the carpet, for example) generates enough electrostatic to damage the ESD.
- Do not take a new ESD from the protective case until the ESD is ready to be installed. Most ESD have a lead, which is easily short-circuited by conductive materials (such as conductive foam and aluminum)

3.NAME & FUNCTION**3-1 Layout of Assemblies**

No.	Location	Name
1	SMPS	SMPS
2	LOGIC-MAIN Board	ASSY PCB LOGIC MAIN
3	X-MAIN Driving Board	ASSY PCB X MAIN
4	Y-MAIN Driving Board	ASSY PCB BY MAIN
5	LOGIC E BUFFER Board	ASSY PCB BUFFER
6	LOGIC F BUFFER Board	ASSY PCB BUFFER
7	Y-BUFFER (UPPER) Board	ASSY PCB BUFFER
8	Y-BUFFER (DOWN) Board	ASSY PCB BUFFER
9	LOGIC + Y-MAIN	FFC CABLE-FLAT
10	LOGIC + X-MAIN	FFC CABLE-FLAT
11	LOGIC + LOGIC BUF(E)	FFC CABLE-FLAT
12	LOGIC + LOGIC BUF(F)	FFC CABLE-FLAT
13	LOGIC BUF(E) + LOGIC BUF(F)	LEAD CONNECTOR
14	SMPS + LOGIC BUF(E)	LEAD CONNECTOR
15	SMPS + LOGIC MAIN	LEAD CONNECTOR
16	SMPS + Y-MAIN	LEAD CONNECTOR
17	SMPS + X-MAIN	LEAD CONNECTOR

**1. SMPS****2. L-Main****3. X-Main****4. Y-Main****5. Y-Buffer (Upper)****6. Y-Buffer (down)****7. E-Buffer****8. F-Buffer**

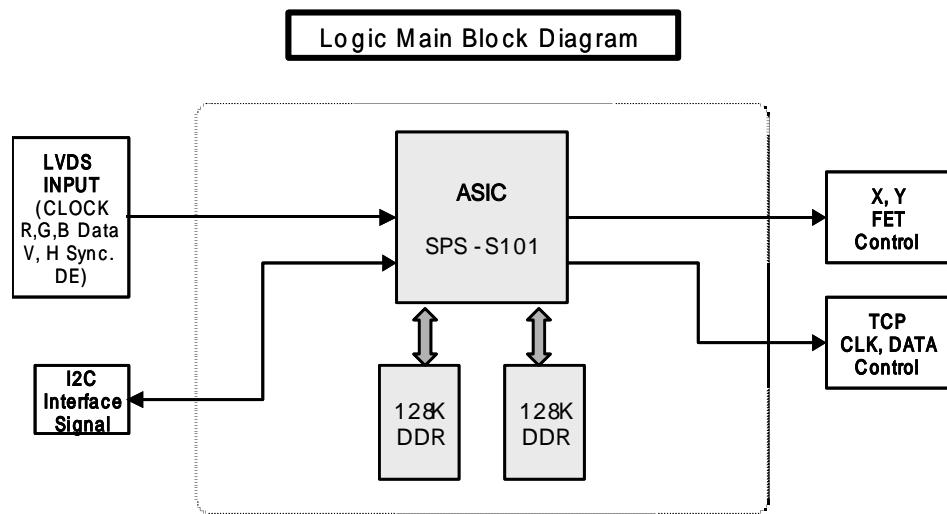
**9. Logic + Y-Main****10. Logic + X-Main****11~12. LOGIC + LOGIC BUF****13. LOGIC BUF(E) + LOGIC BUF(F)**

3-2 BLOCK DIAGRAM

3-2-1 BLOCK DIAGRAM FOR DRIVE CIRCUIT OPERATION

To be Updated

3-2-2 Block Diagram for Logic circuit



3-3 Main function of Each Assembly

X-main board : The X-main board generate a drive signal by switching the FET in synchronization with logic main board timing and supplies the X electrode of the panel with the drive signal through the connector.

- 1) Maintain voltage waveforms (including ERC)
- 2) Generate X rising ramp signal
- 3) Maintain Ve bias between Scan intervals

.Y-main board : The Y-main board generate a drive signal by switching the FET in synchronization with the logic Main Board timing and sequentially supplies the Y electrode of the panel with the drive signal through the scan driver IC on the Y-buffer board. This board connected to the panel's Y terminal has the following main functions.

- 1) Maintain voltage waveforms (including ERC)
- 2) Generate Y-rising Falling Ramp
- 3) Maintain V scan bias

Logic main board : The logic main board generates and outputs the address drive output signal and the X ,Y drive signal by processing the video signals. This Board buffers the address dirve output signal and feeds it to the address drive IC (TCP module)

(video signal- X Y drive signal generation , frame memory circuit / address data rearrangement)

.Logic buffer(E,F) : The logic buffer transmits data signal and control signal.

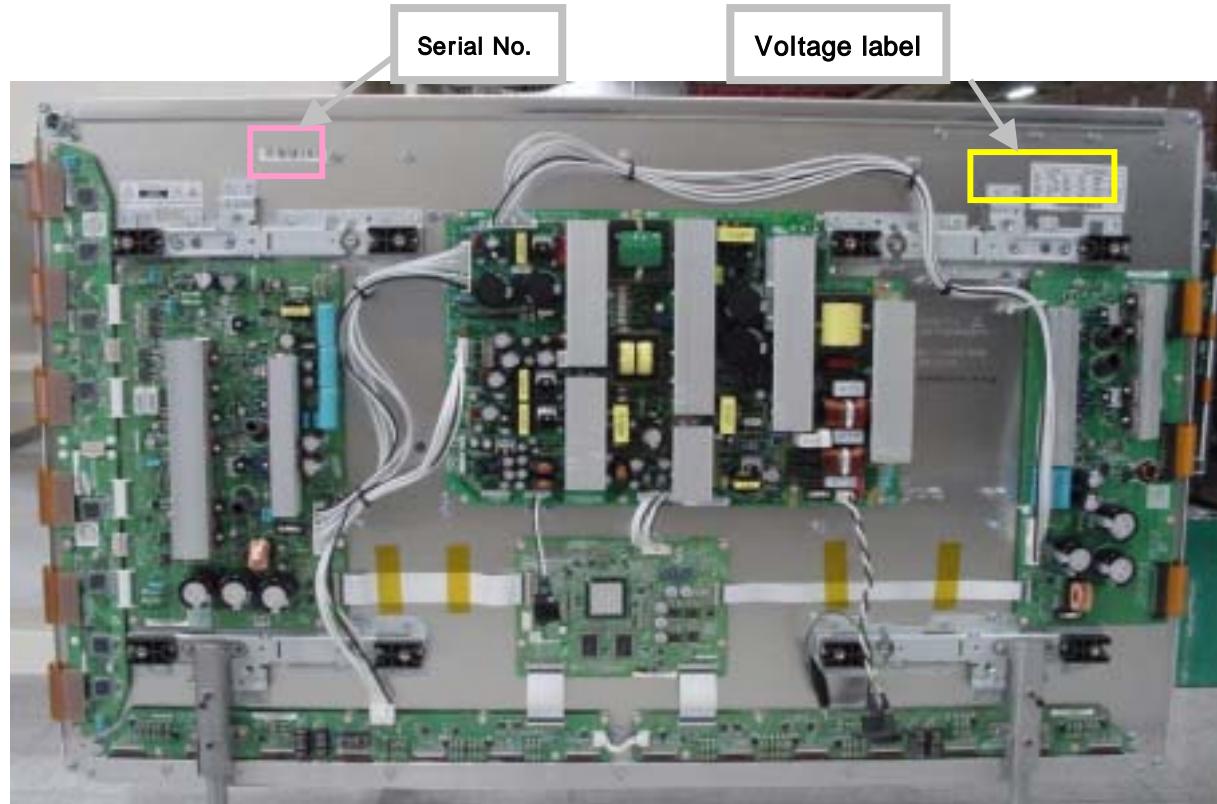
.Y-buffer board (Upper, Lower) : The Y-buffer board consisting of the upper and lower boards supplies the Y-terminal with scan waveforms. The board comprises 8 scan driver IC's (ST microelectronics **STV 7617** : 64 or 65 output pins) , but 4 ICs for the SD class

.AC Noise Filter : The AC Noise filter has function for removing noise(low Frequency) and blocking surge.

It effects Safety standards(EMC,EMI)

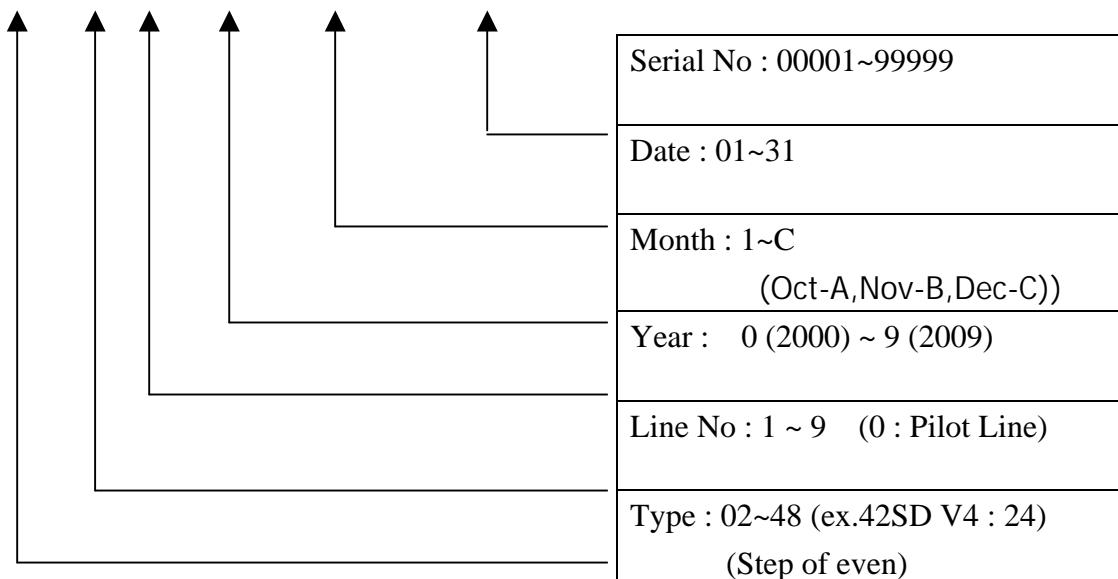
.TCP(Tape Carrier Package) : The TCP applies Va pulse to the address electrode and constitutes address discharge by the potential difference between the Va pulse and the pulse applied to the Y electrode. The TCP comprise 2 data driver Ics(**STV7620A :96 pins output pins**) 14 TCPs are required for signal scan

3-4 PRODUCT/ SERIAL LABEL LOCATION



3-4-1 Serial No.

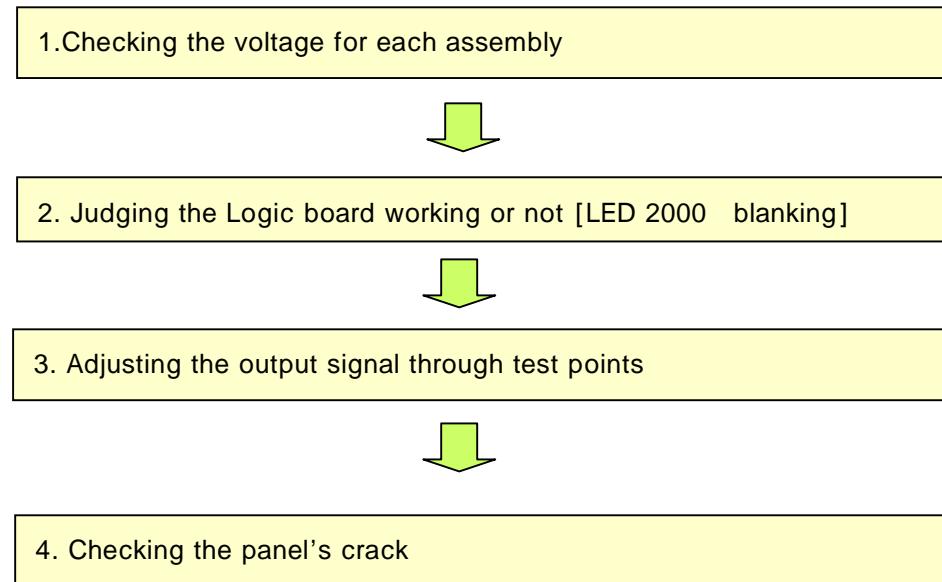
* PANEL S/N

2 4 2 4 C 0 1 0 0 0 1

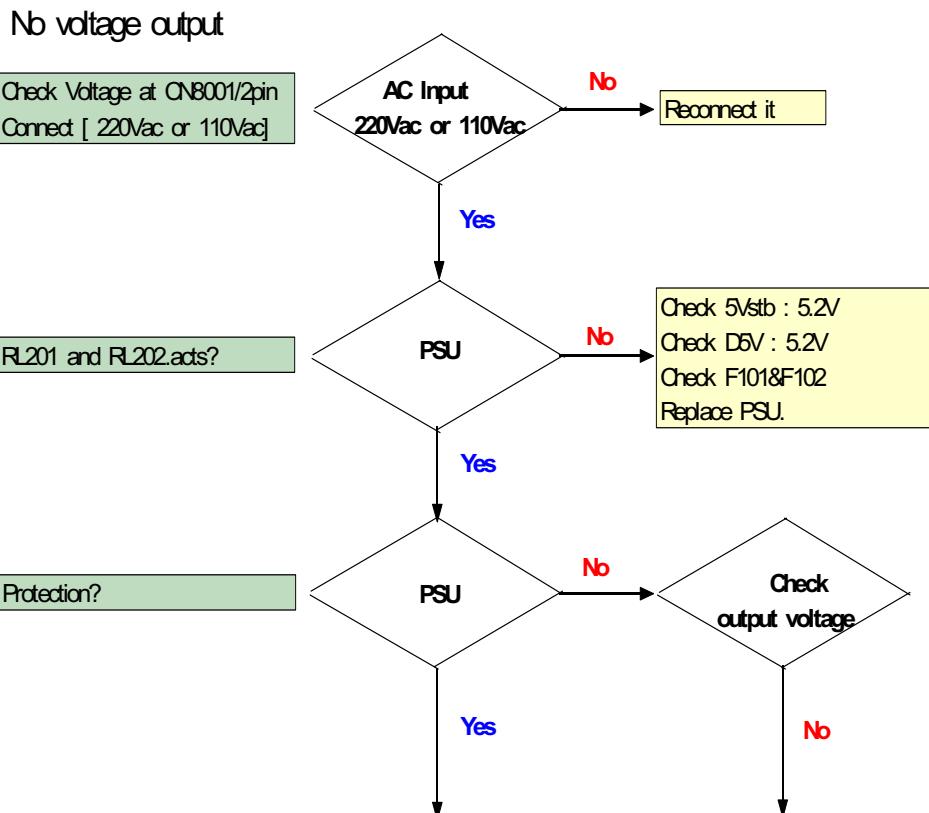
4. OPERATION CHECKING AFTER RECTIFICATION

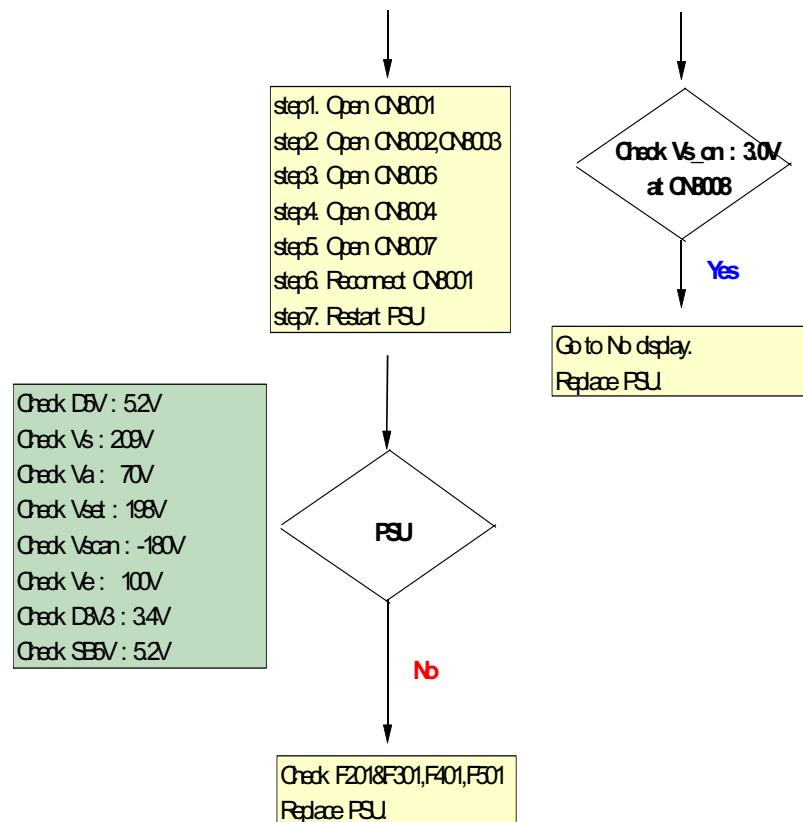
4-1 Flow chart

* A/S Check Point *



4-1-1 No voltage output

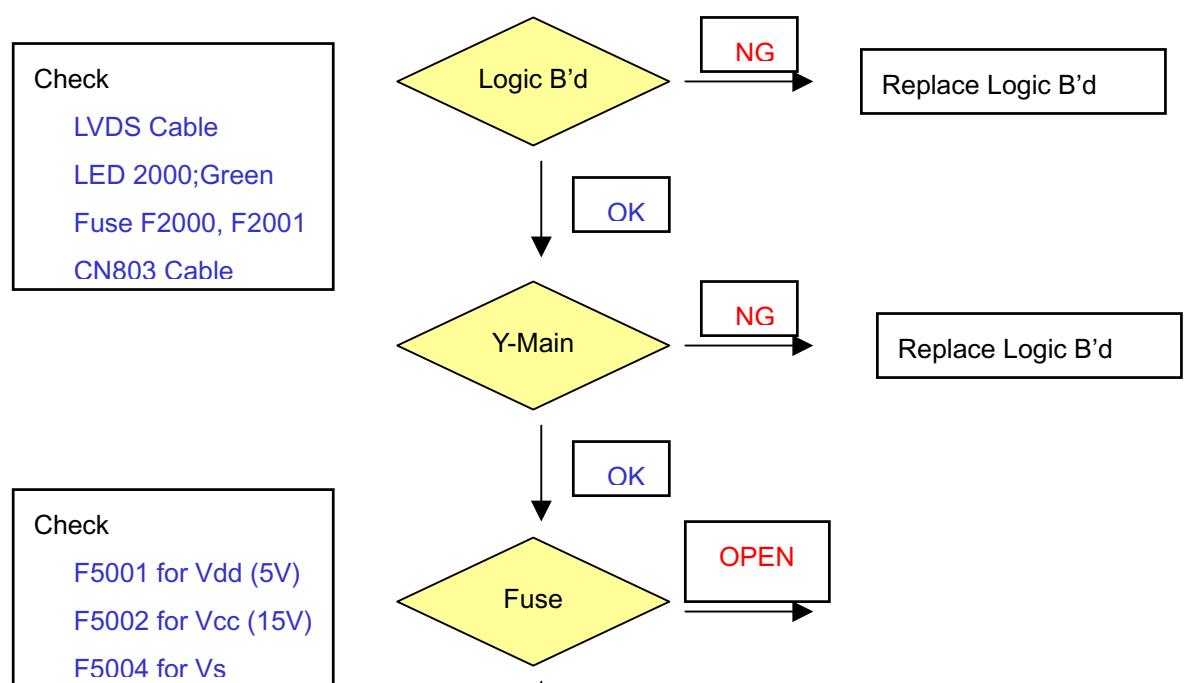
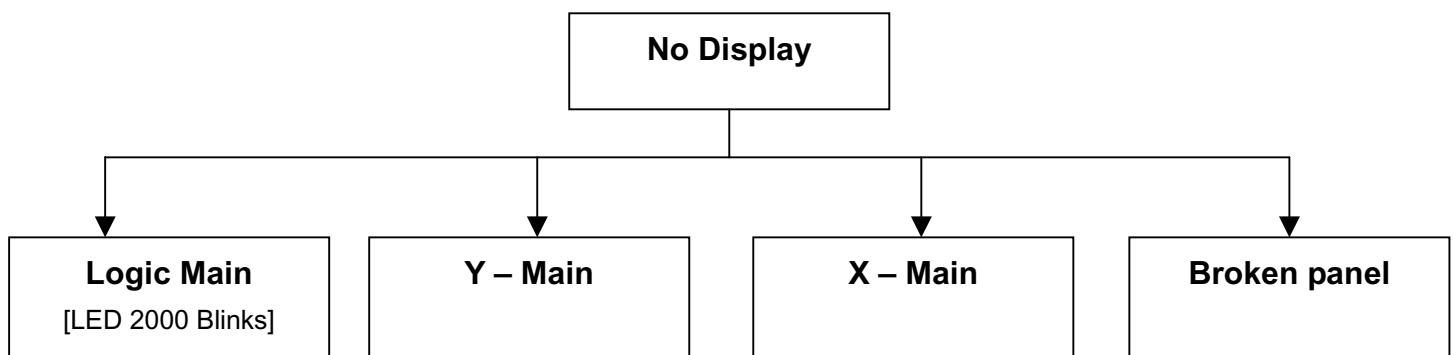




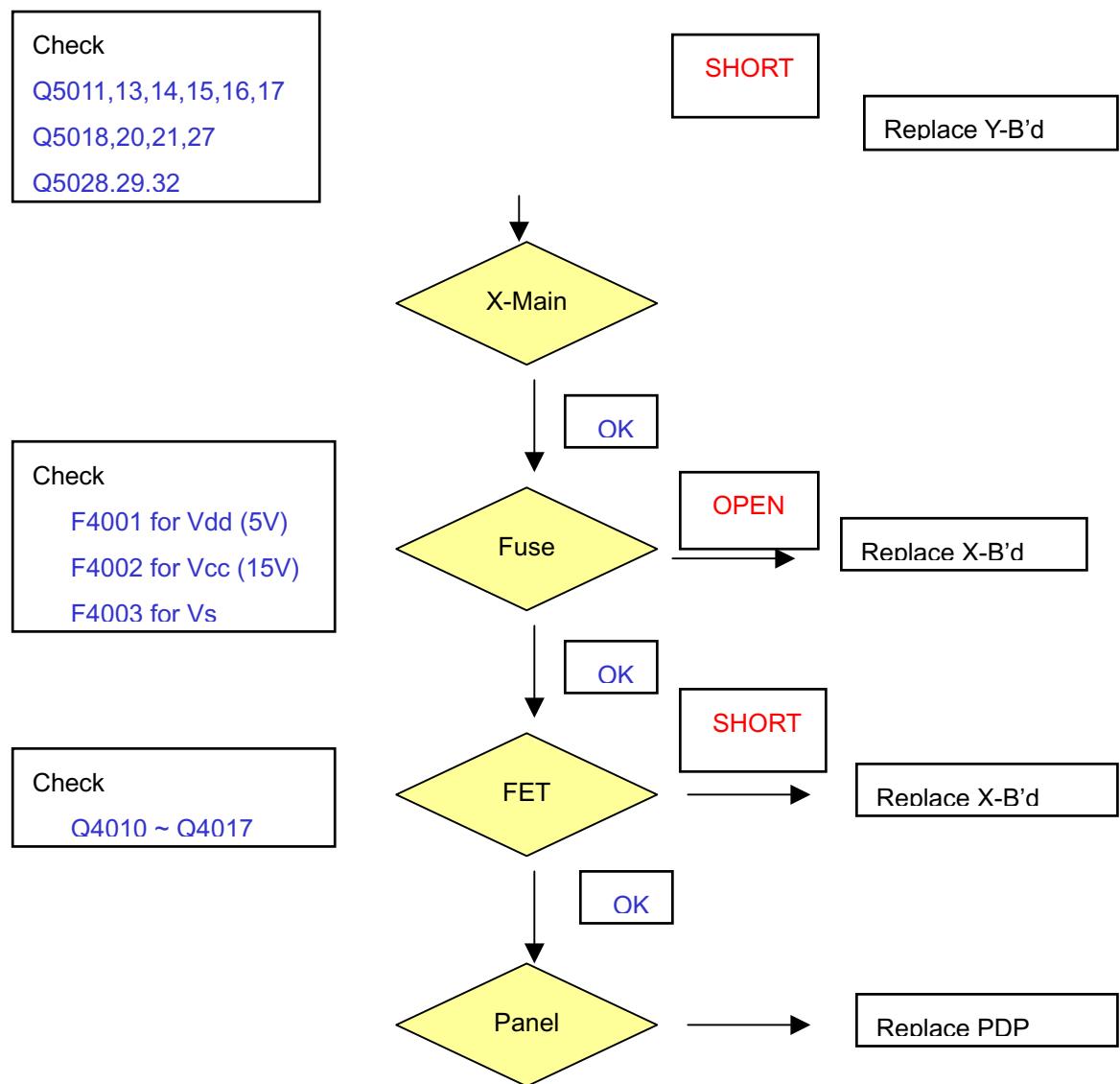
4-1-2 NO display (operating Voltage but an image doesn't exist on Screen)

No Display is related with Y-MAIN, X-MAIN, Logic Main and so on.

This page shows you how to check the boards, and the following pages show you how to find the defective board.



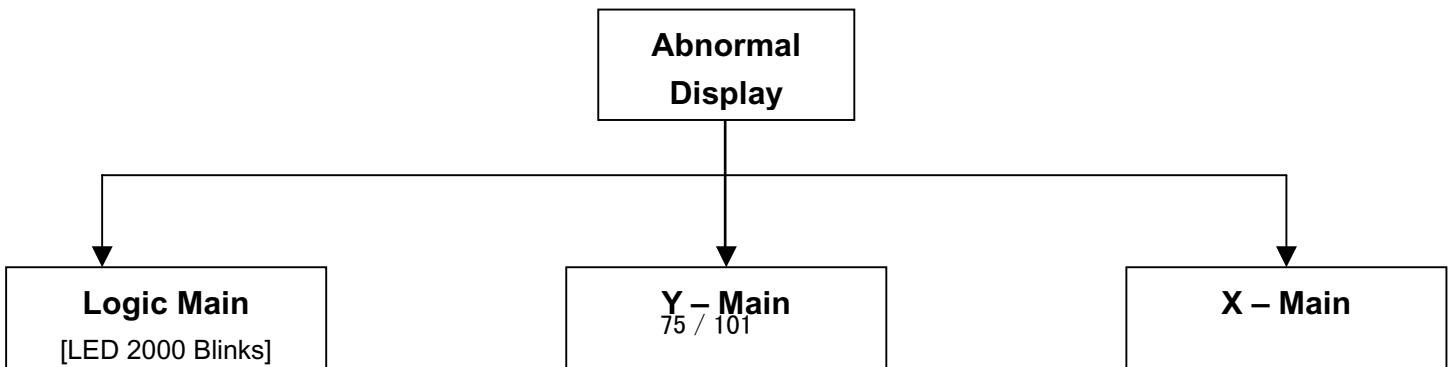
Replace Y-B'd

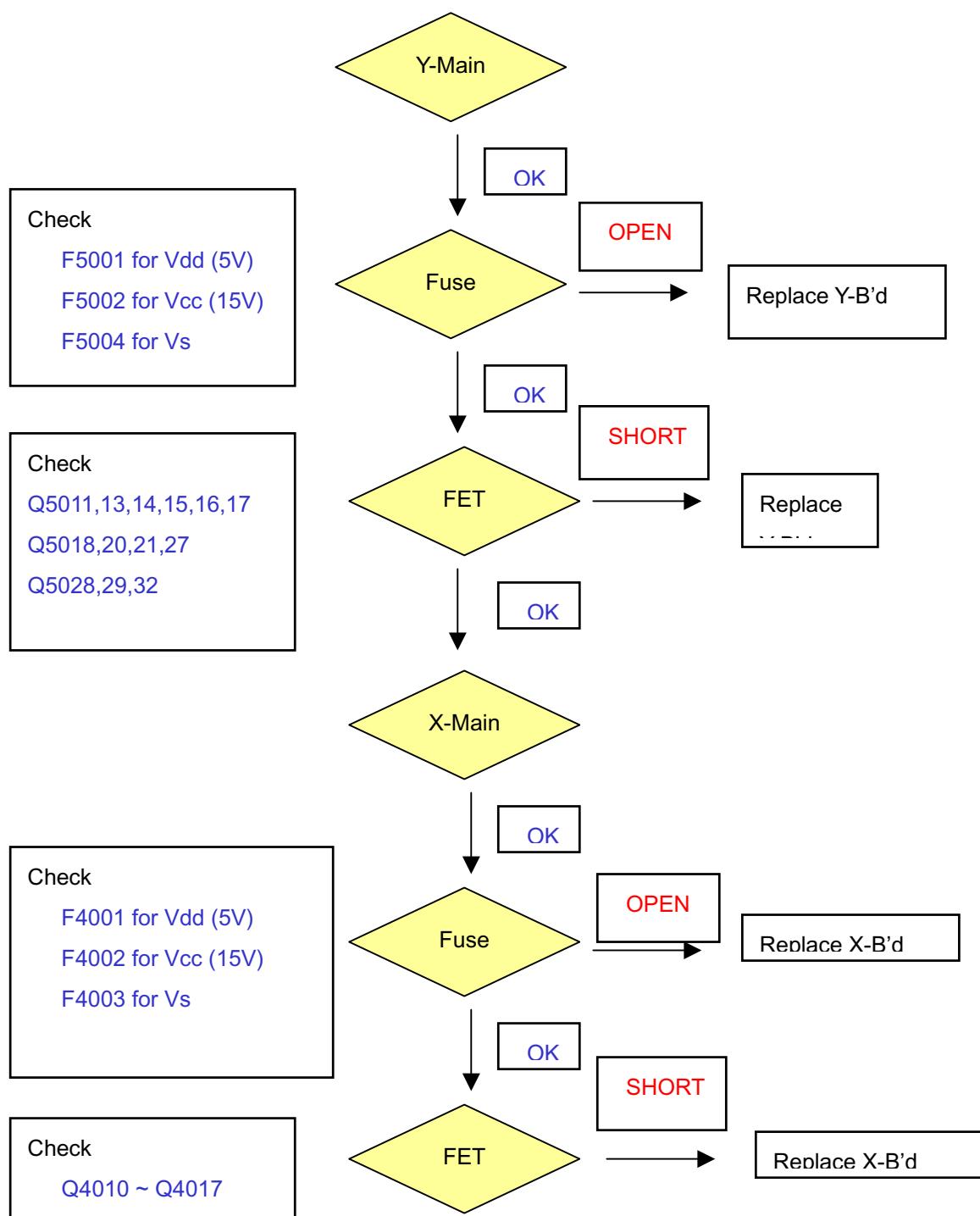


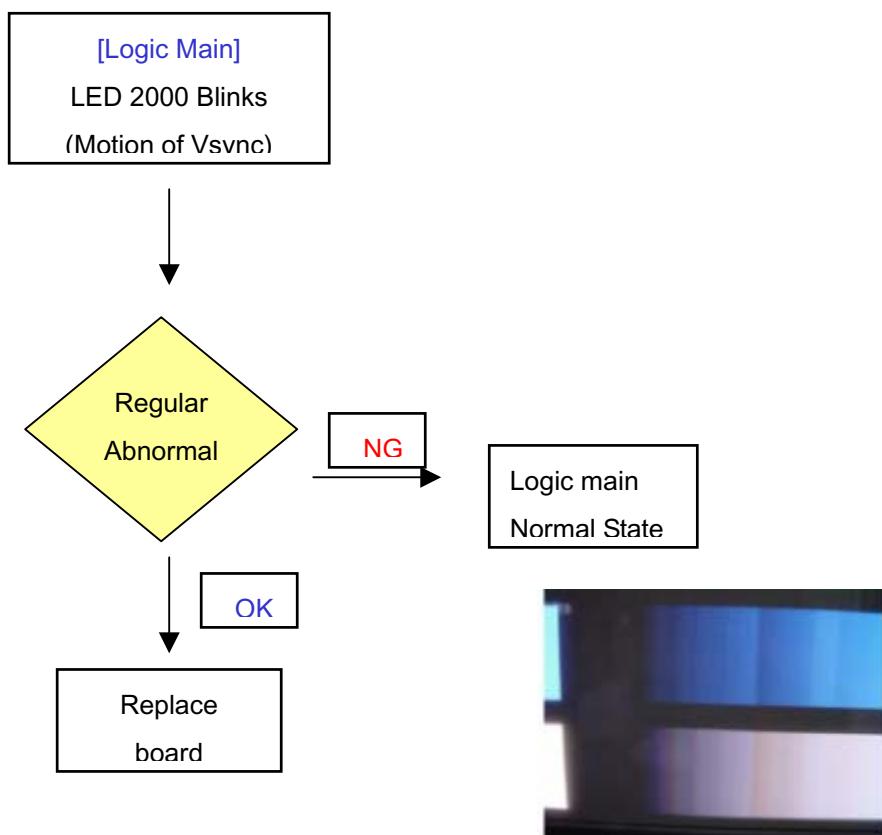
4-1-3 Abnormal Display (Abnormal Image is on Screen. (except abnormality in Sustain or Address))

Abnormal Display is related with Y-MAIN, X-MAIN, Logic Main and so on.

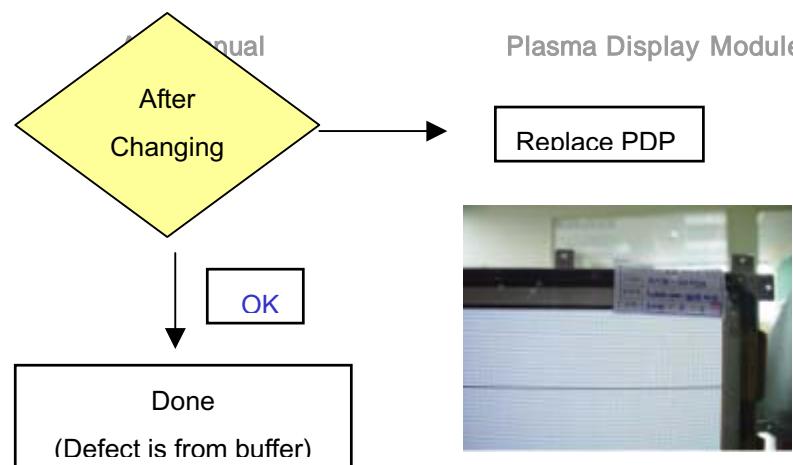
This page shows you how to check the boards, and the following pages show you how to find the defective board.



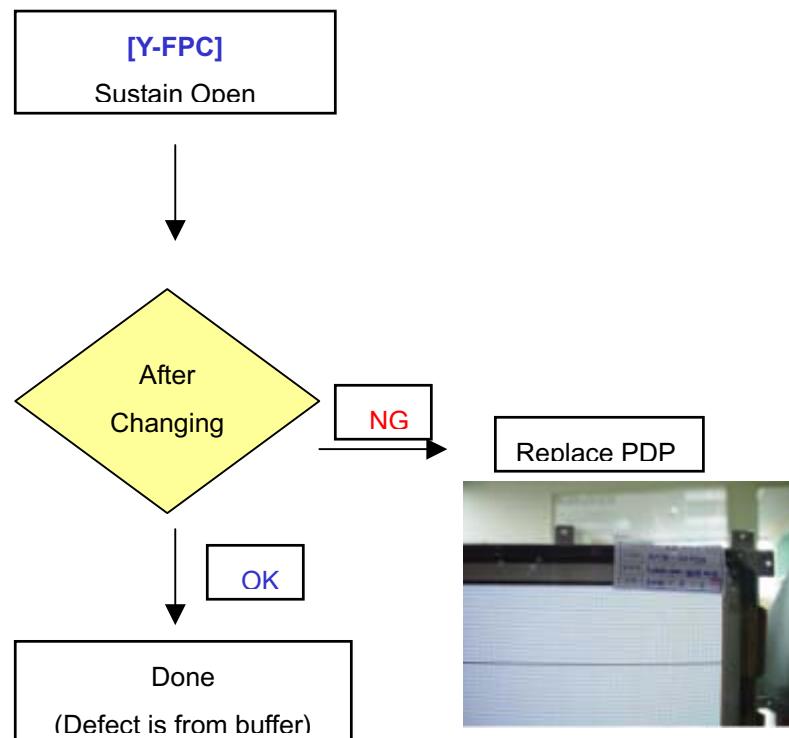


**4-1-4 Sustain Open (some horizontal lines don't exist on screen)**

NG



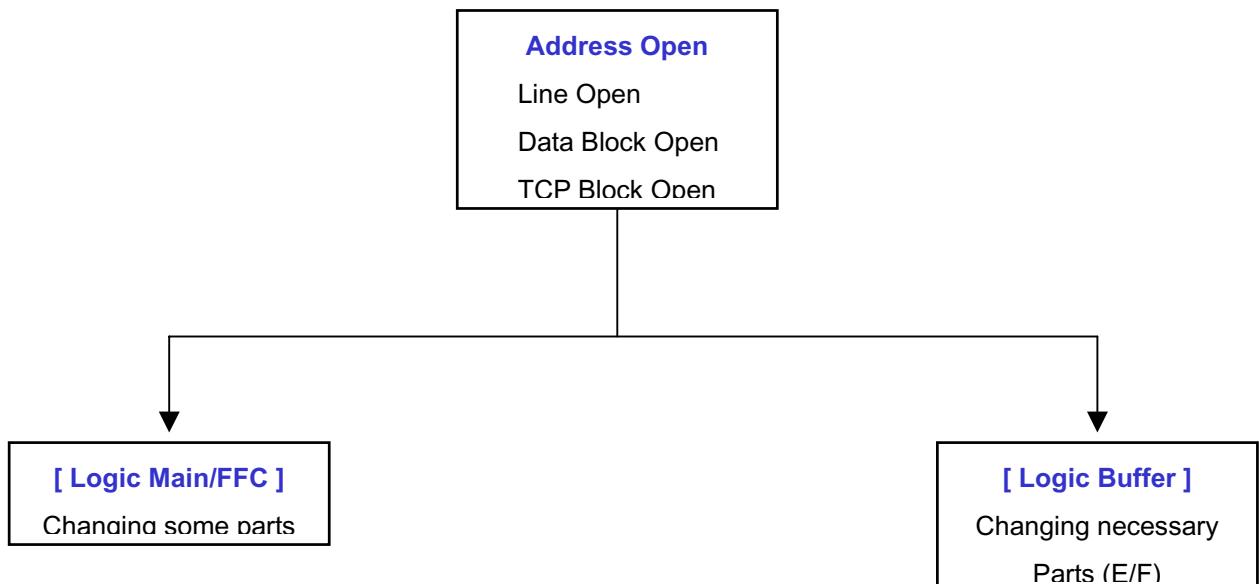
4-1-5 Sustain Short (some horizontal lines appear to be linked on Video)

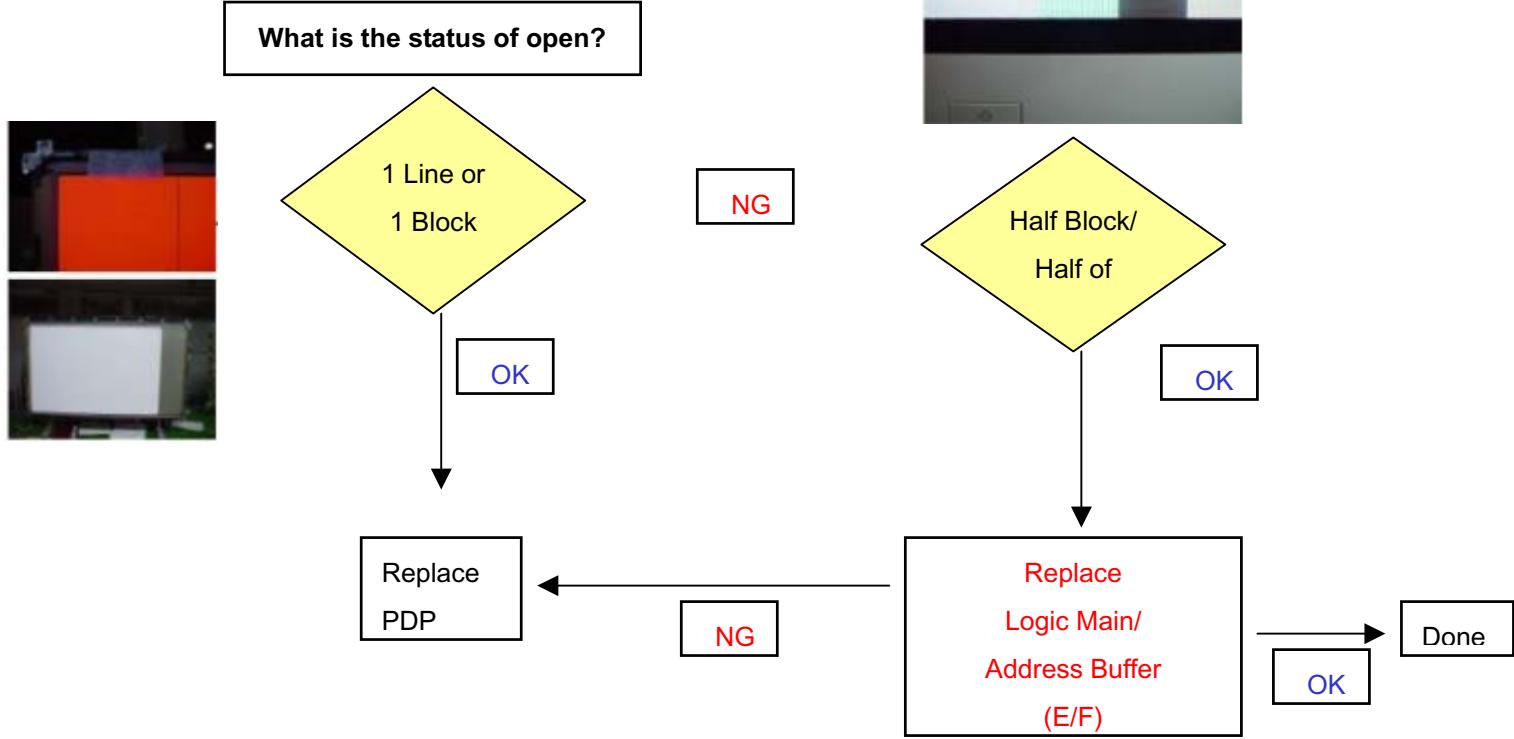


4-1-6 Address Open (some vertical lines don't exist on screen)

Address Open is related with Logic Main, Logic Buffer, FFC, TCP and so on.

This page shows you how to check the boards, and the following pages show you how to find the defective board.

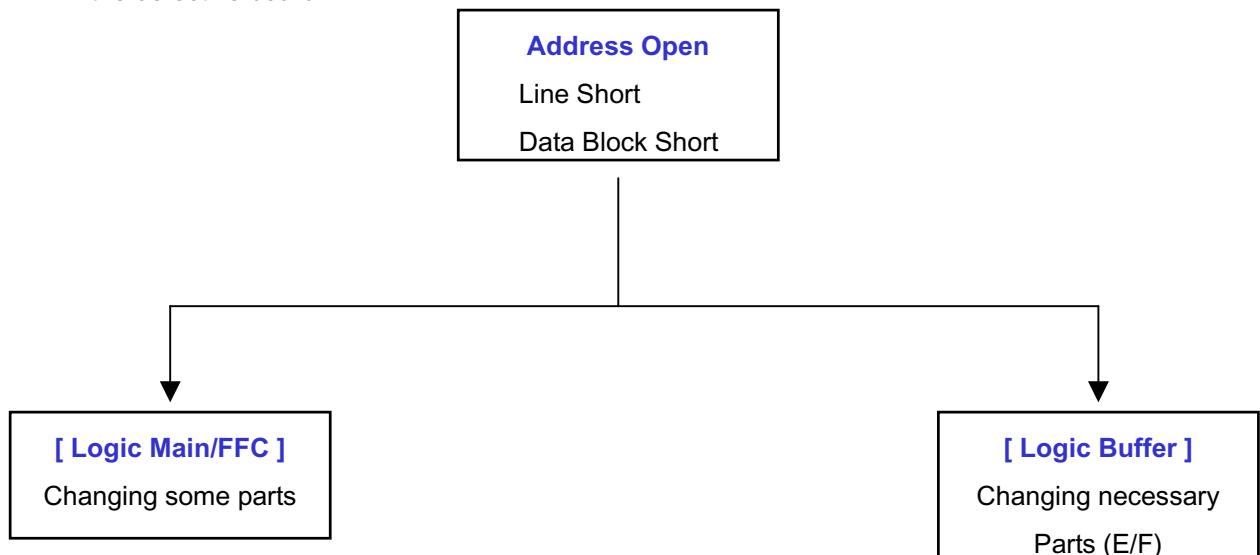


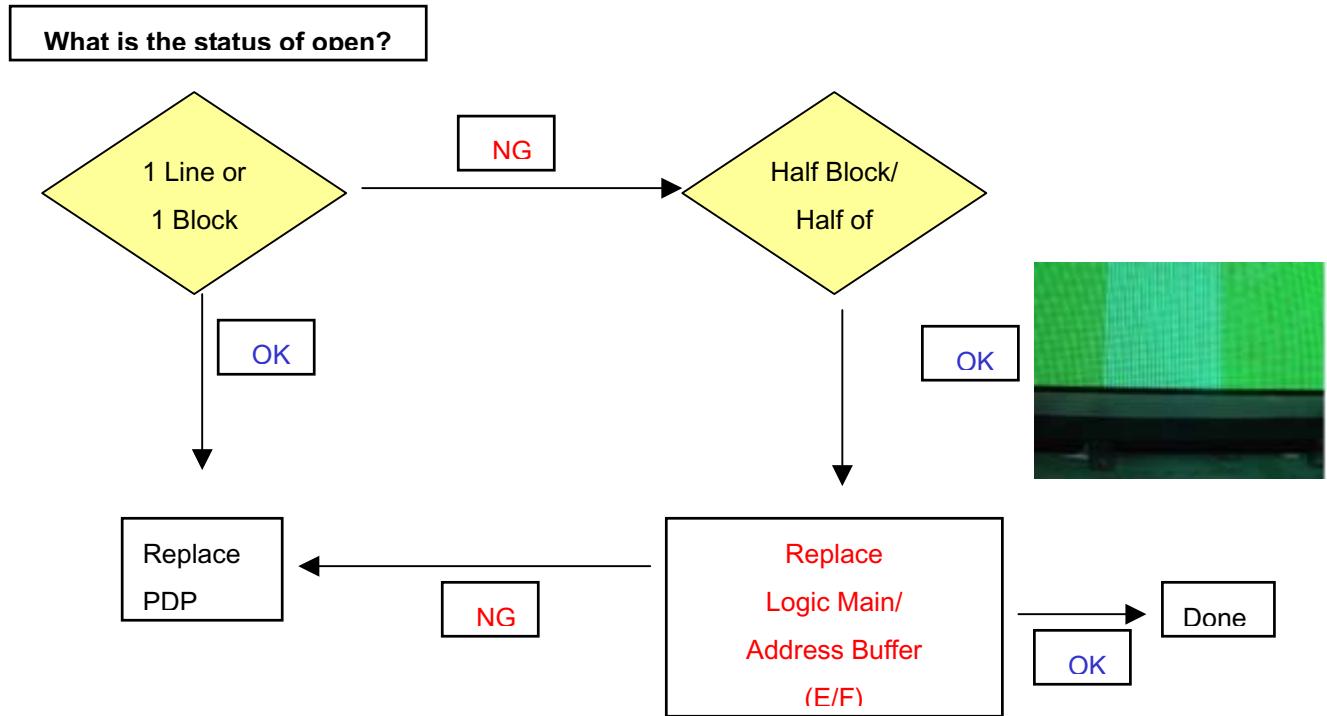


4-1-7 Address Short (some vertical lines appear to be linked on screen)

Address Short is related with Logic Main, Logic Buffer, FFC, TCP and so on.

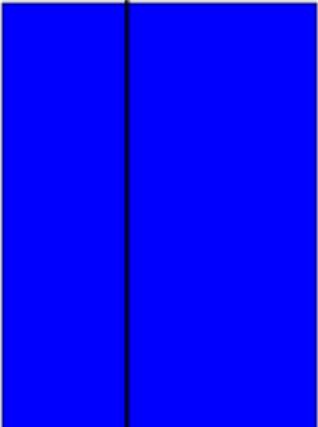
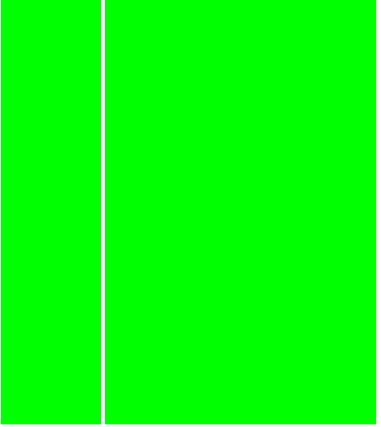
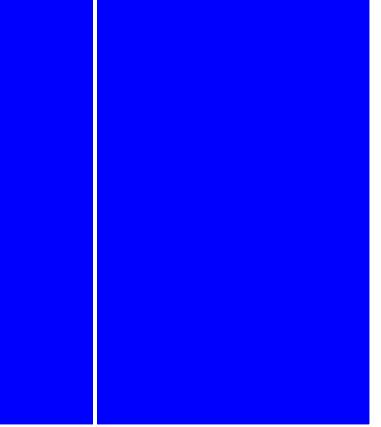
This page shows you how to check the boards, and the following pages show you how to find the defective board.

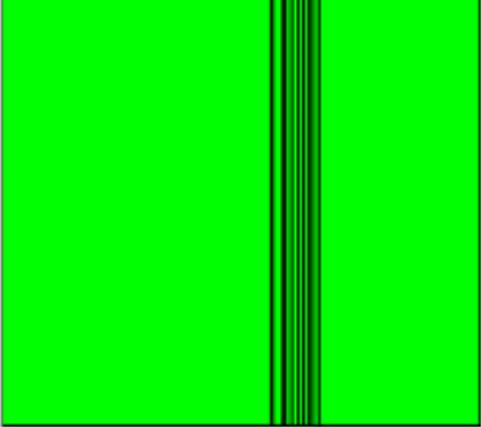
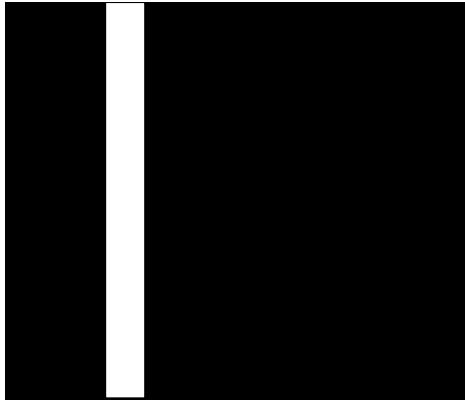
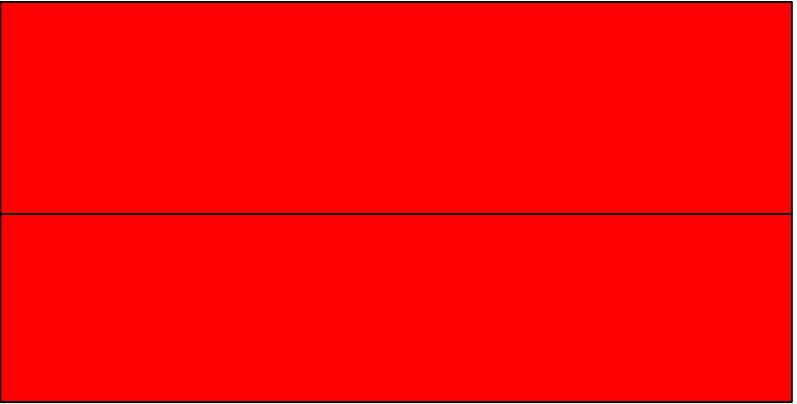


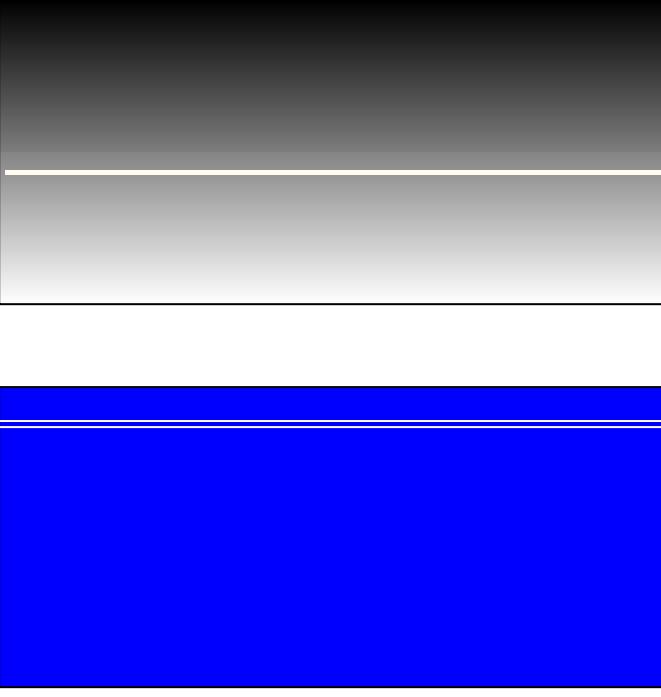
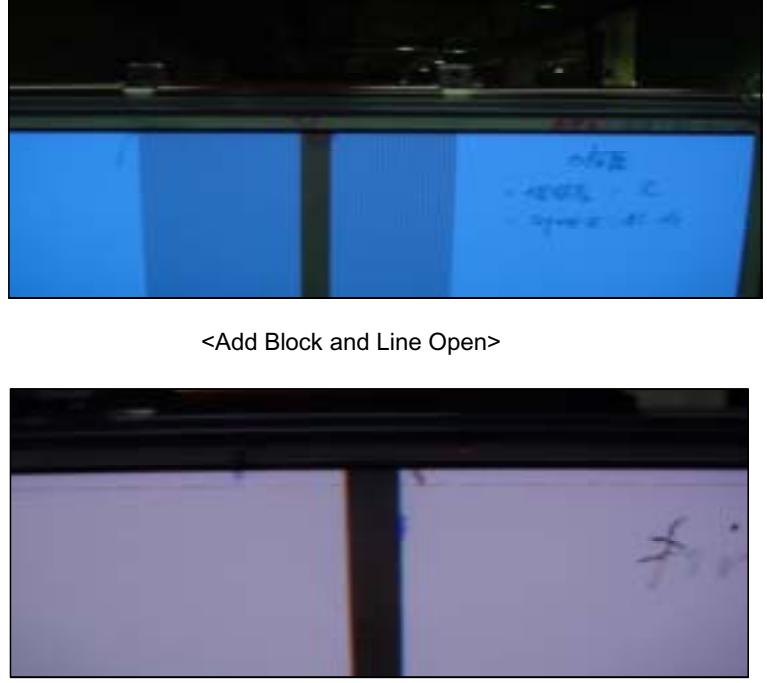


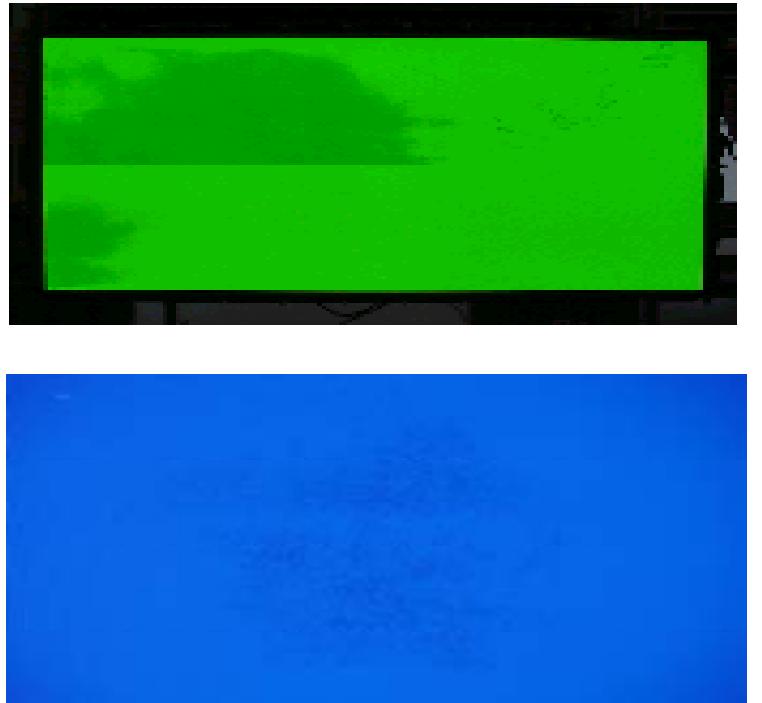
4-2 DEFECTS, SYMPTOMS AND DETECTIVE PARTS

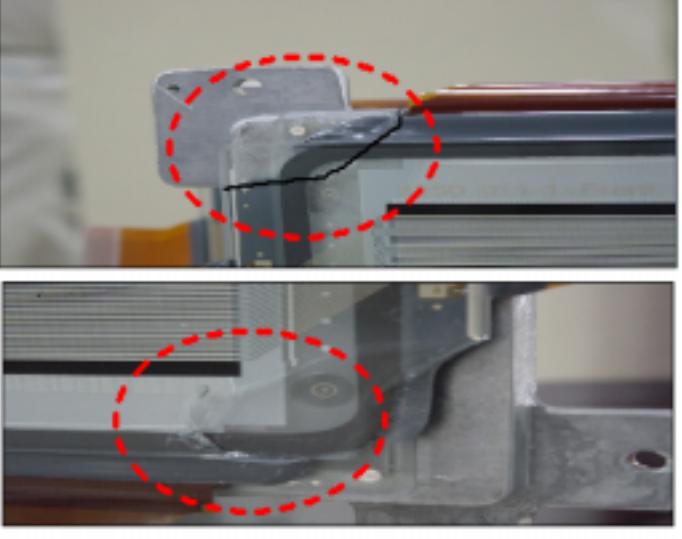
Condition Name	Description	Related Board
No Voltage Output	Operating Voltages don't exist.	SMPS
No Display	Operating Voltages exist, but an Image doesn't exist on screen	Y-MAIN, X-MAIN, Logic Main, Cables
Abnormal Display	Abnormal Image(not open or short) is on screen.	Y-MAIN, X-MAIN, Logic Main
Sustain Open	some horizontal lines don't exist on screen	Scan Buffer, FPC of X / Y
Sustain Short	some horizontal lines appear to be linked on screen	Scan Buffer, FPC of X / Y
Address Open	some vertical lines don't exist on screen	Logic Main, Logic Buffer, FFC,TCP
Address Short	some vertical lines appear to be linked on screen	Logic Main, Logic Buffer ,FFC,TCP

Defect: Address(vertical stripe) Open	Defect: Address(vertical stripe) Short
<p>Symptom : A line or block does not light up in address electrode direction.(1 line ,block open)</p>  	<p>Symptom: Another color simultaneously appears because adjacent data recognizes the single pattern signal</p>  
<p>Cause</p> <p>manufacturing : Panel electrode single line/ foreign material./electrostatic/ TCP defect</p> <p>Parts : TCP, Board connection defect</p> <p>Operation : Assembly error / Film damage</p>	<p>Cause</p> <p>manufacturing : Panel electrode short / Foreign material conductive foreign object inside TCP</p> <p>Part : TCP/buffer defect lighting electrode cutting defect</p>

Defect: Address output error	Defect: Sustain(horizontal stripe) Open
<p>Symptom.: A defect other than address open and short Data printout signal error occurring at certain Gradation or pattern</p>  	<p>Symptom : One or more line do not light up in Sustain direction</p>  <p>Cause : manufacturing : .Panel bus electrode single line FPC pressure defect Parts : FPC/board/connection disconnection operation : assembly error.</p>

Defect: Sustain(horizontal stripe) Short	Defect: Dielectric material layer damage
<p>Symptom : Combined or adjacent lines are short in sustain direction. The line appear brighter than other at Ramp gradation pattern or low gradation patter</p> 	<p>Symptom: Burn caused by the damage of address bus dielectric layer appears in the panel discharge/non discharge area. sustain also open/short occurs by the damage of address sustain printout</p>  <p><Add Block and Line Open></p>
<p>Cause</p> <p>manufacturing : Panel electrode short/Foreign material.</p> <p>Parts : Board/ connector/pin error</p> <p>Operation : connector / assembling error</p>	<p><Add and Sustain Open></p> <p>Cause : layer uneven / abnormal voltage / foreign material repair failed</p>

Defect: F/White low discharge	Defect: Weak discharge
<p>Symptom : Low discharge caused by unstable cells occurring at full white pattern if high (60 degree) or normal temperature.</p> 	<p>Symptom : Normal discharge but cells appear darker due to weak light emission occurring mainly at low (5 degree) Full white/Red/Green/Blue pattern or gradation pattern</p> 
<p>Cause</p> <p>Panel : MgO source / dielectric thickness cell pitch/phosphor</p> <p>Circuit : drive waveform/ voltage condition</p>	<p>Cause</p> <p>Panel : MgO deposition count and thinckness / aging condition</p> <p>Circuit : drive waveform/ voltage condition</p>

Defect : panel damage	Defect: Exhaust pipe damage
<p>Symptom : Panel crack or break. No image appears in some cause depending on the damaged parts and damage level.</p> 	<p>Symptom. : Crack in break if exhaust pipe an image is partially lacking or the panel noise occurs depending on the damaged parts and with the passage of time</p> 
<p>Cause</p> <p>Manufacturing : Flatness/palette pin interruption</p> <p>Operation : overload of panel corner / careless handling</p> <p>Panel : Flatness / assembly error</p>	<p>Cause : Careless panel handling</p>

5. Disassembling / Assembling

5-1 Tools and measurement equipment

5-1-1. Tools

- 1) (+) type Screw Drivers : to screw the screws
- 2) Air Blower
- 3) Earth Ring
- 4) Small Driver : to adjust potentiometer
- 5) Dummy Discharge Resistor : 2.4kOhm/10W

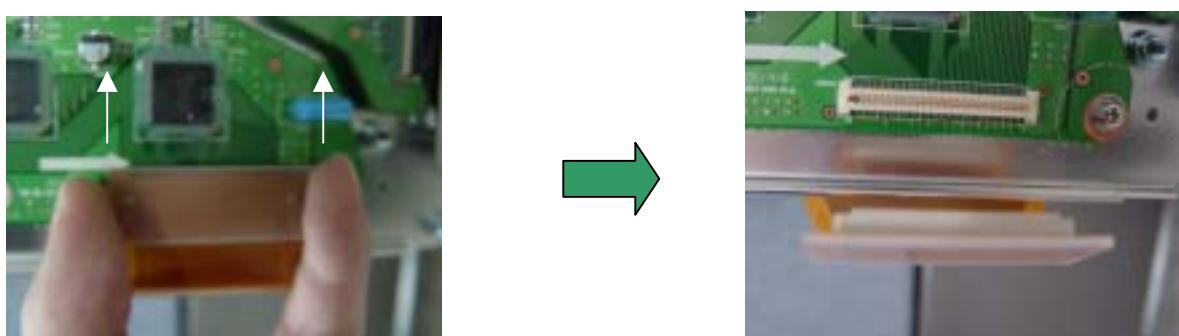
5-1-2. Measuring Equipment

- 1) Oscilloscope : 500MHz sampling
- 2) Probe : 10:1
- 3) Digital Multi-meter
- 4) Signal Generator

5-3 Disassembling & Re-assembling

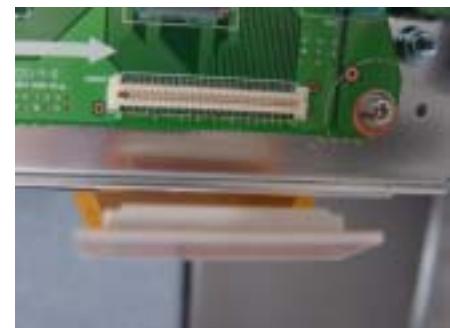
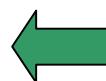
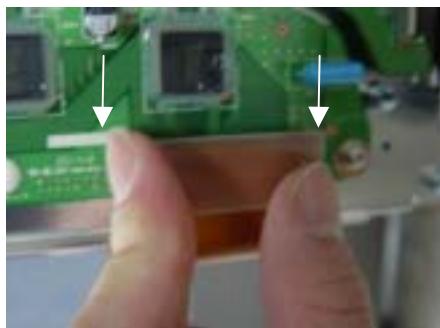
5-3-1 Disassembling & Re-assembling of FPC (Flexible Printed Circuit) and Y-Buffer(Upper and Lower)

1. Removal procedures



- 1) Full out the FPC from Connector by holding the lead of the FPC with hands.

2. Assembling Procedures

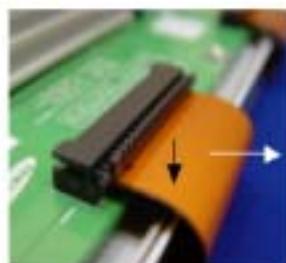


- 1) Push the lead of FPC with same strength until to be connected completely.

* Notice : Be careful do not get a damage on the connector pin during connecting by mistake.

5-3-2 Assembling & Disassembling of Flat Cable Connector of X-Main Board

1. Disassembling Procedure

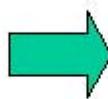
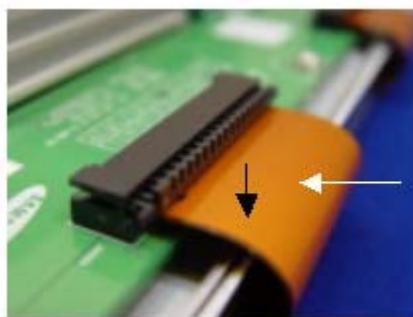


- 1) Pull out the clamp of connector.

- 2) Pull Flat cable out press down lightly.

- 3) Turn the Flat cable reversely.

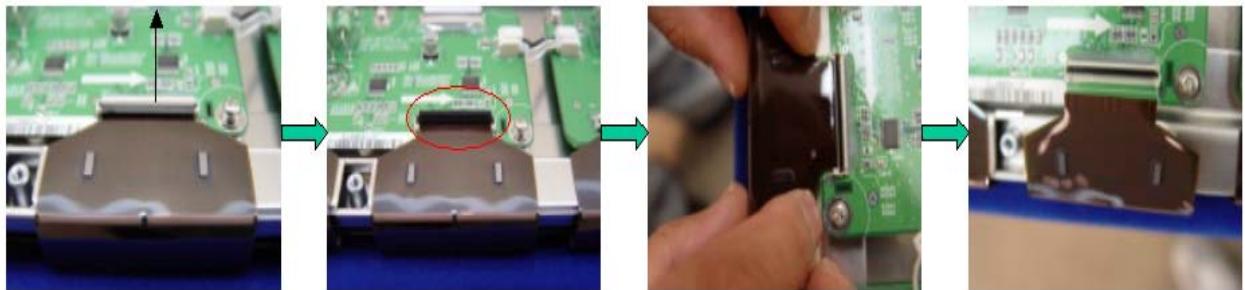
2. Assembling Procedure



- 1) Put the Flat cable into the connector press down lightly until locking sound ("Dack") comes out.

5-3-3 Assembling & Disassembling the FFC and TCP from Connector

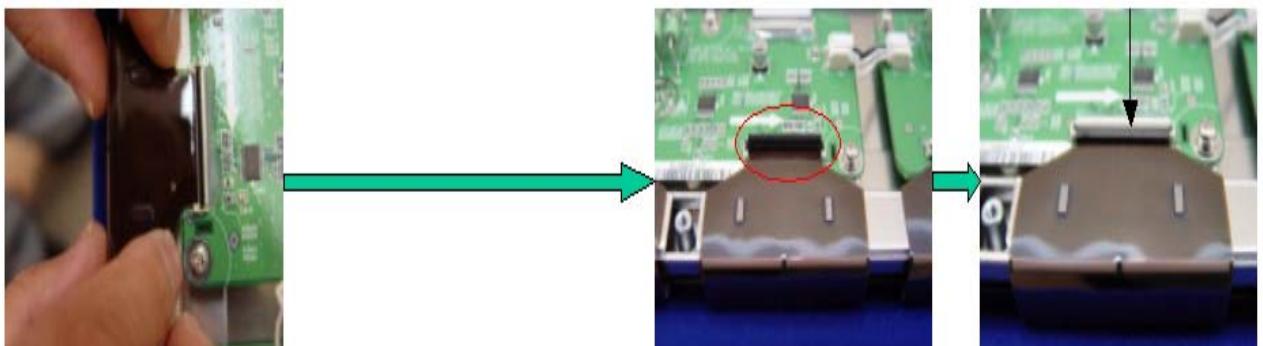
1. Disassembling of TCP



1) Open the clamp carefully.

2) Pull the TCP out from Connector.

2. Assembling of TCP



1) Put the TCP into the Connector carefully

2) Close the clamp completely.

(The sound (" Dack") comes out.)

* Notice : TCP and Connector was connected surely.

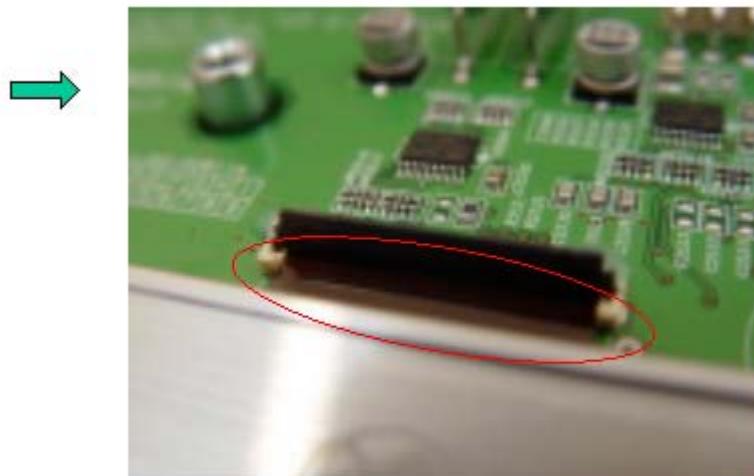
* Notice :

1) Checking whether the foreign material is on the Connector inside before assembling of TCP.

2) Be careful do not get a damage on the board by ESD during handling of TCP.

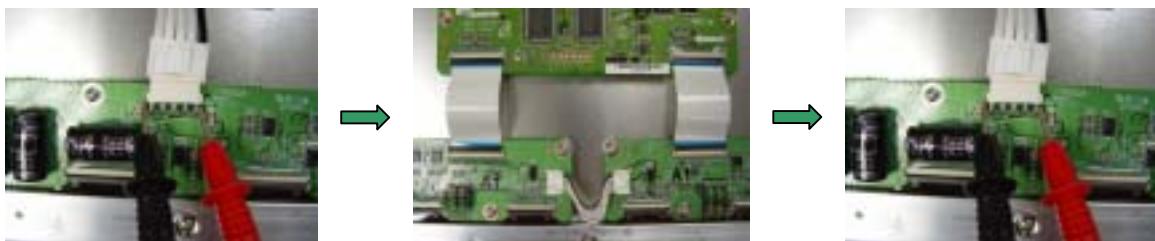
3. Misassembling of TCP

- 1) The misassembling of TCP is the cause of defect.

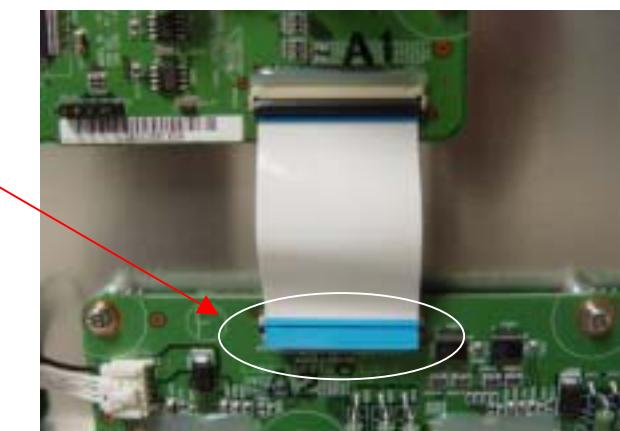


4. Checking method of misassembling of TCP

- 1) Disconnecting address harness from CN8006 of LBE.

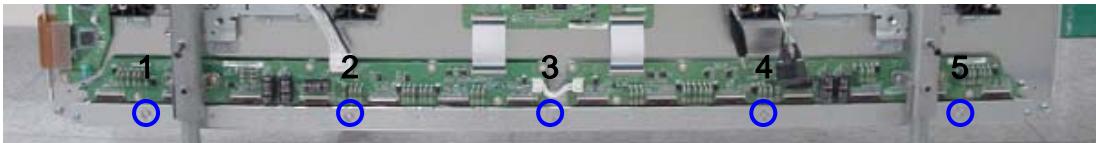


5. Assembling & Disassembling of FFC

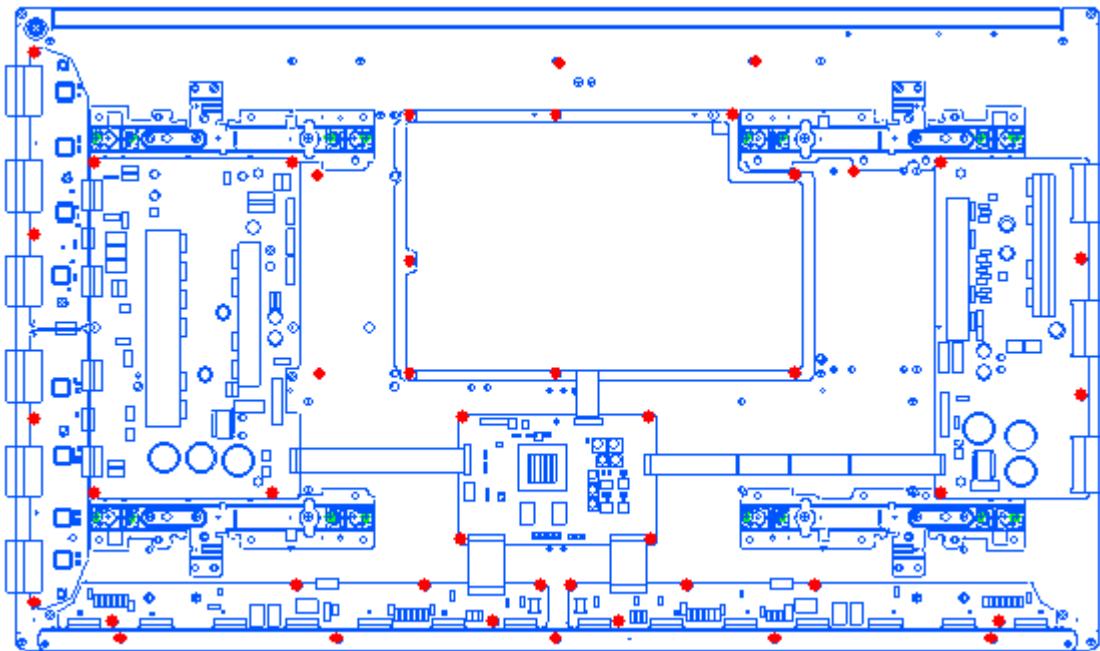


(This is the photo of the assembling of FFC)

The procedure of assembling and disassembling of FFC is the same as TCP.

5-3-4 Exchange of LBE, LBF board

(Photo 1)



(Photo 2)

- 1) Remove the screws in order of 2-4-1-5-3 from heat sink and then get rid of heat sink. (Photo 1)
- 2) Remove the TPC, FFC and power cable from the connectors.
- 3) Remove all of the screws from defected board.
- 4) Remove the defected board.
- 5) Replace the new board and then screw tightly.
- 6) Get rid of the foreign material from the connector.
- 7) Connect the TCP, FFC and power cable to the connector.
- 8) Reassemble the TCP heat sink.
- 9) Screw in order of 3-1-5-2-4. (Photo 2)

If you screw too tightly, it is possible to get damage on the Driver IC of TCP.

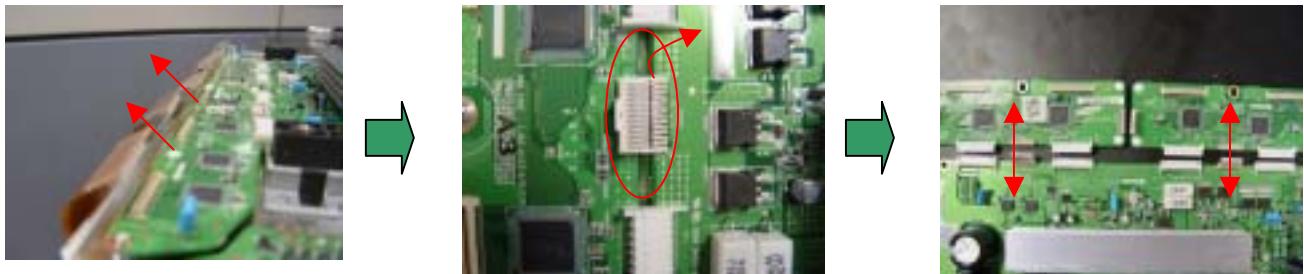
5-3-5 Exchange YBU, YBL and YM board

- 1) Separate all of the FPC connector of YBU (Y-Buffer upper) and YBL (Lower). (Photo 1)
- 2) Separate all of the connector of CN5003 and CN5004 from Y-Main. CN5407 from YBU and YBL
- 3) Loosen all of the screws of YBU, YBL and YM.
- 4) Remove the board from chassis.

5) Remove the connector of CN5005, CN5006, CN5007 and CN5008 among YBU, YBL and YM.

6) Remove the YBL and YBU from Y-main.

7) Replace the defected board.



8) Reassemble the YBU and YBL to the Y-Main.

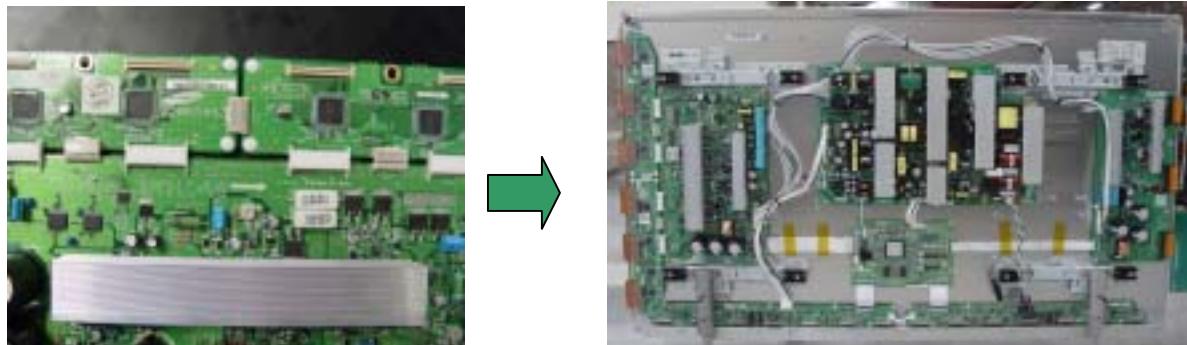
9) Connect the connector of CN5005, CN5006, CN5007 and CN5008 among YBU, YBL and YM.

10) Arrange the board on the chassis and then screw to fix.

11) Connect the FPC and YM of panel to the connector.

12) Supply the electric power to the module and then check the waveform of board.

13) Turn off the power after the waveform is adjusted.



6. Operation Check after Repair Service

6-1 Check Item

	Check Item	Specification	Remarks
Module assemble check	TCP Assembling condition	Securely connected or tightened	
	Drive board		
	Y BUFFER		
	Logic & Logic Buffer		
	Harness	Securely connected	
	Material Mixing	No material mixing	

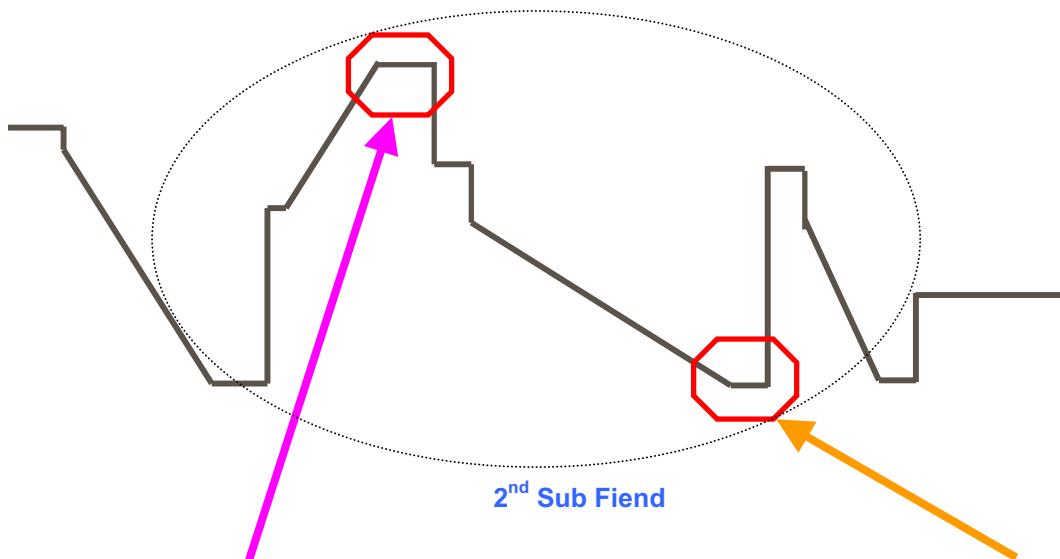
6-2 Check Procedure

- 1) Visual check as following
 - a. Assembling condition of module.
 - b. No problem on the connection of module.
 - c. The grounding and easily short-circuited parts are not damaged.
- 2) Turn on the power to PDP module, and then check that LED lights up and the SET is working well.
- 3) Check the power voltage after turn on the power, and then check the Display condition by tapping slightly the Y-FPC 2 or 3 times.
- 4) Check whether something wrong during Full White Pattern period.
- 5) If something wrong, each voltage should be set to the standard voltage by using Multi-Tester and adjusting tools.
- 6) Adjust the waveform, using Oscilloscope for the waveform adjusting point.
- 7) Check the discharge of front panel by changing the image for each pattern.
- 8) Check the Low-discharge, Over-discharge and panel condition by adjusting the Pattern Generator Level.
- 9) Discharge still remain send back to SDI

7. Operation Check

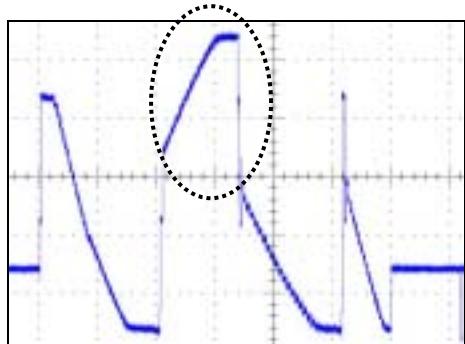
7-1 Adjustment Specification, Checking Position etc.

V4 TCP Ramp Waveform Inclination Adjustment (Y-Board)

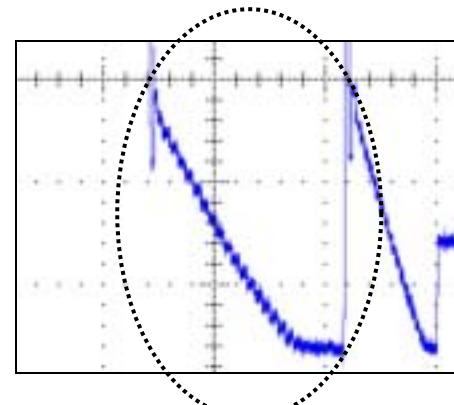


Adjust VR5001 to set the time of
Yrr(Main Reset Rising Ramp) **60μs**

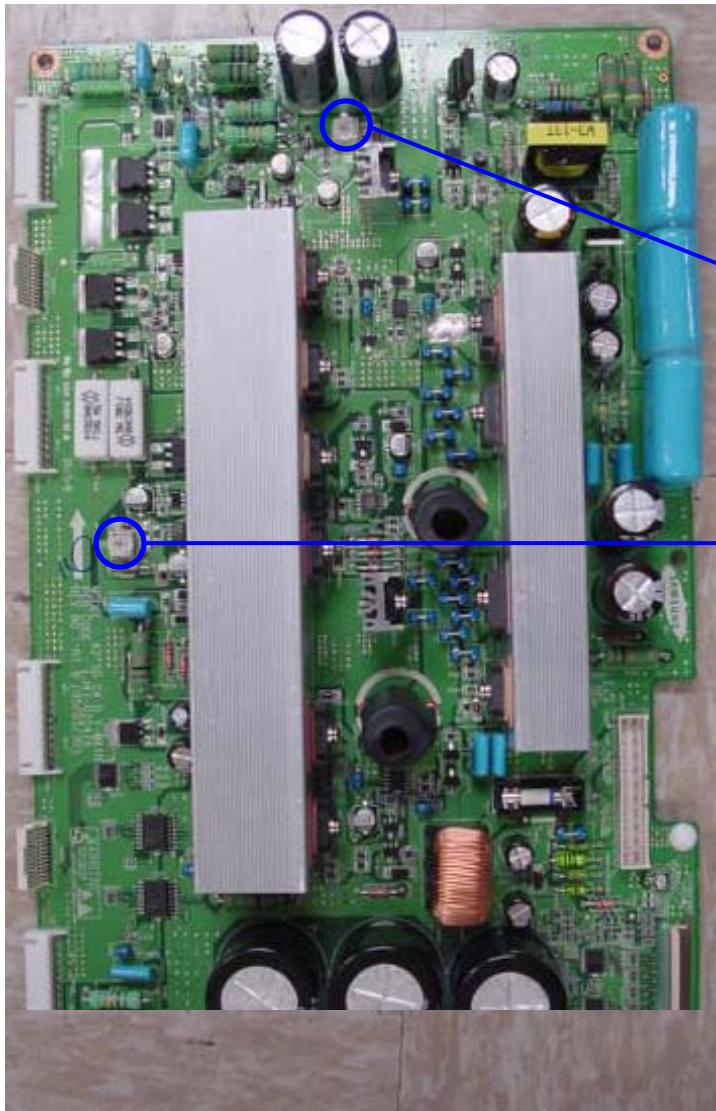
Adjust VR5003 to set the time of
Yfr (Main Reset Falling Ramp) **80μs**



< Rising Ramp >



< Falling Ramp >



VR5003 Adjustment :
Falling Ramp flat time => Typ. 80usec

VR5001 Adjustment :
Rising Ramp flat time: Typ. 60usec

7-2 Adjusting procedure

1) 1) Get Pattern to be Full White.

2) Check the waveform using Oscilloscope

Triggering through V_TOGG of LOGIC Board.

Connect the OUT240 Test Point at the center of Y_buffer to other channel, and then check the 2nd SF operating waveform of 1TV-Field.

Check the waveform as before by adjusting Horizontal Division.

Check the Reset waveform when the V_TOGG Level is changed.

Set the Vset to **60us** by adjusting VR5001.

Set the Falling maintenance time to **80us** by adjusting R5003.

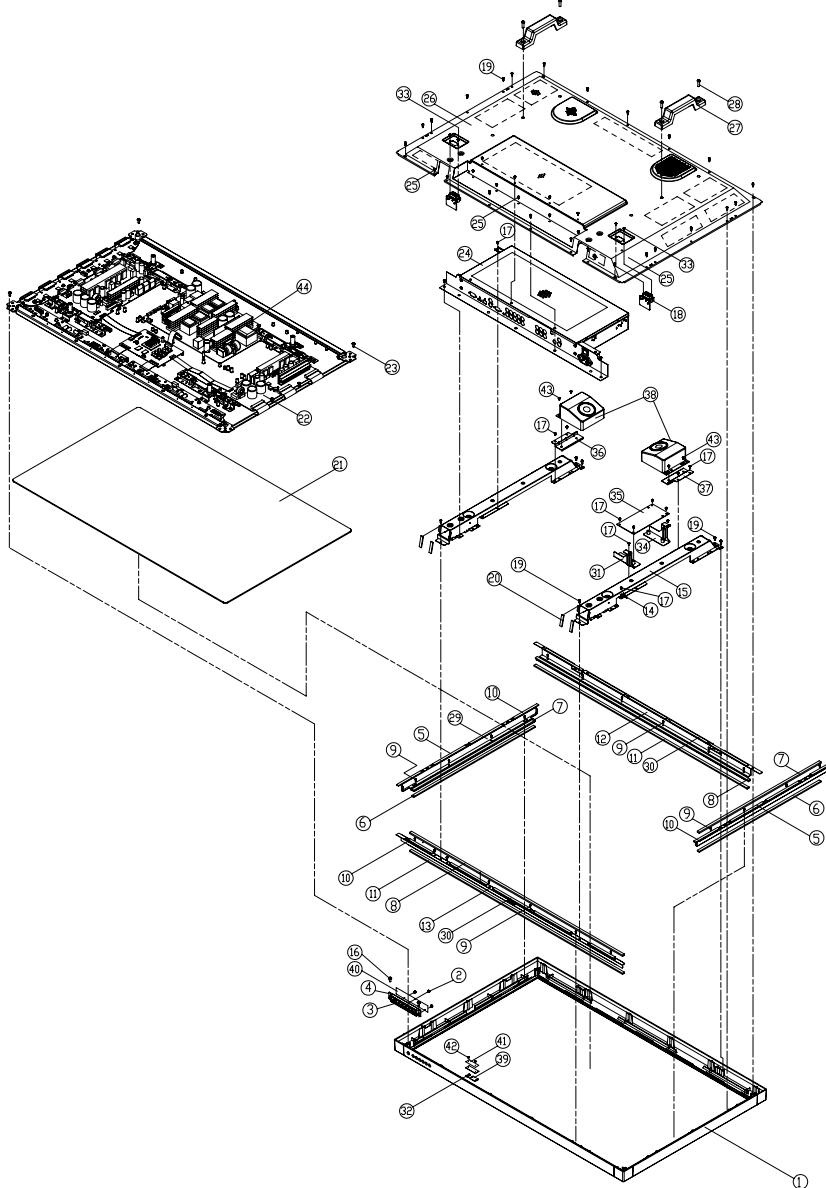
Appendix 1. Adjust Voltage Level

No	Output voltage(V)	Voltage Setting (Normal Load)	Output Voltage Variable Point
1	VS	207V \pm 1%	195V ~ 215V
2	VA	70V \pm 1.5%	50V ~ 70V
3	VE	110V \pm 1.5%	70V ~ 110V
4	VSET	198V \pm 1.5%	180V ~ 210V
5	VSCAN	-185V \pm 1.5%	-170V ~ -190V
6	VSB	5V \pm 5%	Fixed
7	VG	15V \pm 5%	Fixed
8	D5VL	5.2V \pm 5%	Fixed
9	D3V3	3.3V \pm 5%	Fixed

Item	Part Number	Part Description	Usage / unit	Unit
1	E6205-42SA02	DISPLAY PDP 42"	1	piece
2	900-420101-01B	DISPLAY FILTER 42"	1	piece
3	771E42AA02-04	MAIN PCBA	1	set
4	771L42AA02-04	AUDIO PCBA	1	set
5	771-42AB01-01	KEY PCBA	1	set
6	771-42D110-01	IR RECEIVE PCBA	1	piece
7	E7801-080001	POWER PCBA	1	set
8	771-50AA05-01	SPEAK JACK PCBA	1	set
9	786-SPA103-01	SPK ASSY FOR PD42HAA(LG) 16 OHM 7W R/L=1150MM/800MM EMI	1	set
10	E4101-027001	POWER SWITCH	1	piece
11	E4801-116002	SPEAKER	2	piece
12	E3219-002003	POWER SOCKET	1	piece
13	E3301-017002	TERMINAL PUSH WP2-19	2	piece
14	E3404-157001	AC POWER CORD	1	piece
15	E3421-927006	AMP/AMP -2Y/550 (FROM SWITCH POWER) FOR SDI	1	piece
16	E3421-927021	L=300MM 3WIRES FOR 42EAA POWER CONNECT W/EMI	1	piece
17	E3421-926042	WIRE ASSY 5P 2.54MM L=1150MM/800MM EMI	1	piece
18	E3421-926034	POWER CABLE 2Y/L=300MM FOR (SDI 50") (W/EMI)	1	piece
19	E3421-926041	WIRE ASSY 13P/6P+8P 2.0MM L=500MM KEY/REMOTE (EMI)	1	piece
20	E3421-926077	WIRE ASSY L=245 31P(LVDS W-EMI) FOR 42" SDIV4	1	piece
21	E3421-926069	WIRE ASSY 2.5 8P/10P+4P L=280MM EMI	1	piece
22	E3421-926068	WIRE ASSY 2.5 9P/11P L=190MM EMI	1	piece
23	E3421-926071	WIRE ASSY 4P/3P+3P 2.5MM L=900MM/450MM EMI	1	piece
24	E7501-052001	REMOTE	1	set
25	E7301-010002	AAA SIZE BATTERY	2	piece
26	200-42AA01-SMK01A	FRONT CABINET BLACK	1	piece
27	208-SPA101-01R	SPEAKER BOX TOP CABINET	2	piece
28	209-SPA101-01R	SPEAKER BOX BOTTOM CABINET	2	piece
29	277-42D101-01S	FUNCTION KNOB	1	piece
30	263-42D101-01S	POWER LENS	1	piece

Item	Part Number	Part Description	Usage / unit	Unit
31	269-42D101-01L	IR LENS	1	piece
32	481-50AA03-01S	SHIELD BOX BOTTOM	1	piece
33	483-50AA01-01	SHIELD BOX COVER	1	piece
34	436-42AA07-01S	TERMIAL SHEET	1	piece
35	402-42AA01-01S	BACK COVER	1	piece
36	248-46D201-01	HANDLE FOR PLASMA	2	piece
37	734-BM0501-02	STAND BASE	1	set
38	510-42AA01-SMU01K	CARTON BOX	1	piece
39	518-42AA01-01K	BTM TRAY	1	piece
40	300-42AA03-01C	POLYFOAM SHEET	2	piece
41	300-42AA01-02C	POLYFOAM FOR BTM L&R	1	piece
42	300-42AA02-02C	POLYFOM FOR TOP L&R	1	piece
43	244-34B811-01	GIFT BOX HANDLE	2	piece
44	310-504004-01	MAIN UNIT PLASTIC BAG	1	piece
45	310-151404-01T	INSTRUCTION MANUAL POLYBAG 15"X14"X0.04MM	1	piece
46	580-P42AAES-MU01L	INSTRUCTION MANUAL	1	piece
47	599-BM0502-01	IB SHEET E OF TEARDOWN	1	piece
48	388-42D103-01H	CAUTION LABEL	1	piece
49	388-50AA01-01H	SPEAKER L PLATE ENG (-+)	1	piece
50	388-50AA01-02H	SPEAKER R PLATE ENG (-+)	1	piece
51	387-42AA01-SMU01H	MODEL PLATE	1	piece
52	579-SPA101-15	INT. SPEAKER LABEL FOR 786-SPA103-01 L	1	piece
53	579-SPA101-16	INT. SPEAKER LABEL FOR 786-SPA103-01 R	1	piece
54	384-42AA01-SMU01H	SHEET FOR TERMINAL	1	piece
55	590-42AA01-05	WARRANTY CARD	1	piece
56	593-42AA01-03	INSERTION CARD	1	piece
57	579-42D102-09	SERIAL NO/BAR CODE LABEL	1	piece
58	579-50AA02-01	DANGER CAUTION LABEL	1	piece
59	579-42AA01-07	BAR CODE LABEL	2	piece
60	579-42D105-01	PROTECTIVE EARTH LABEL	1	piece
61	568-P46T02-02	WARNING LB EN	1	piece

EXP 1



If you forget your V-Chip Password

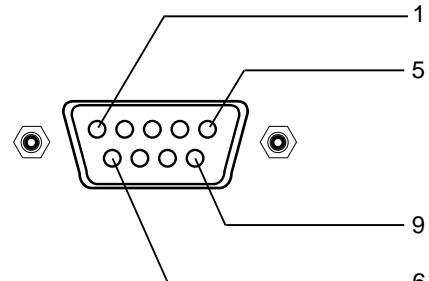
- Omnipotence V-Chip Password: **5898**.
- Press **MENU** button.
- Press **Up, Down** buttons to highlight "V-Chip" Control.
- Press **OK** button to pop up "INPUT PASSWORD".
- Use the Number buttons (0~9) to enter the omnipotence Password 5898.
- Press **Down** to highlight "Password change" Control.
- Press **OK** button to confirm and will pop up "Password Change" item.
- Change to your familiar Password again.

Software upgrade

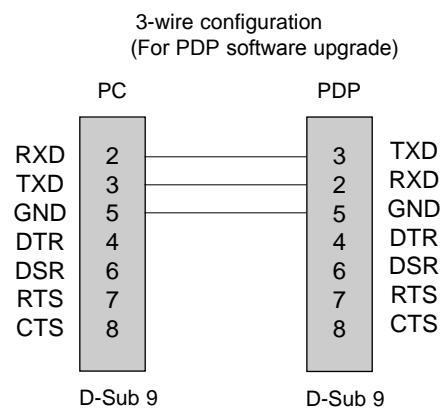
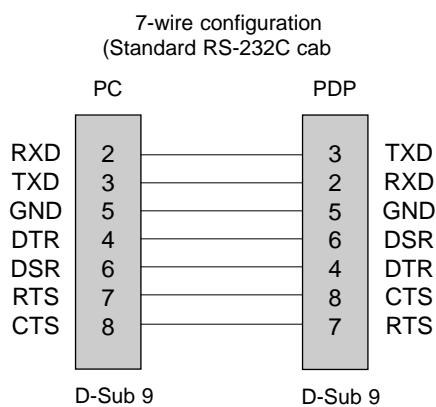
- Connect the RS-232C input jack to an external control device (such as a computer) and software upgrade.

Type of connector; D-Sub 9-pin male

No.	Pin name
1	No connection
2	RXD (Receive data)
3	TXD (Transmit data)
4	DTR (DTE side ready)
5	GND
6	DSR (DCE side ready)
7	RTS (Ready to send)
8	CTS (Clear to send)
9	No Connection



RS-232C configurations



Software upgrade Process

- Power Switch OFF.
- Connect the serial port of the control device to the RS-232 jack on the PDP back panel.
RS-232C connection cables are not supplied with the PDP.
- Power Switch ON. The power indicator on the front of the panel should now display red, means that the PDP is in standby mode.
- Copy the software (Flash Upgrader) to the computer.
- Open the software (Flash Upgrader.exe)
- Point "Flash" on the interface of the Flash Upgrader.exe.
- Press STANDBY button on the front panel or POWER button of Remote control, Power indicator green, the PDP is in power ON mode, software start upgrader immediately.
- Waiting for the upgrader programing, when it is finished, the PDP will auto power on.
- After the upgrader is finished, shut down the power switch, take out the RS-232C connection after the power indicator is extinguished.

Note: The computer and PDP must be keep **Power ON** in the software upgrade processing.